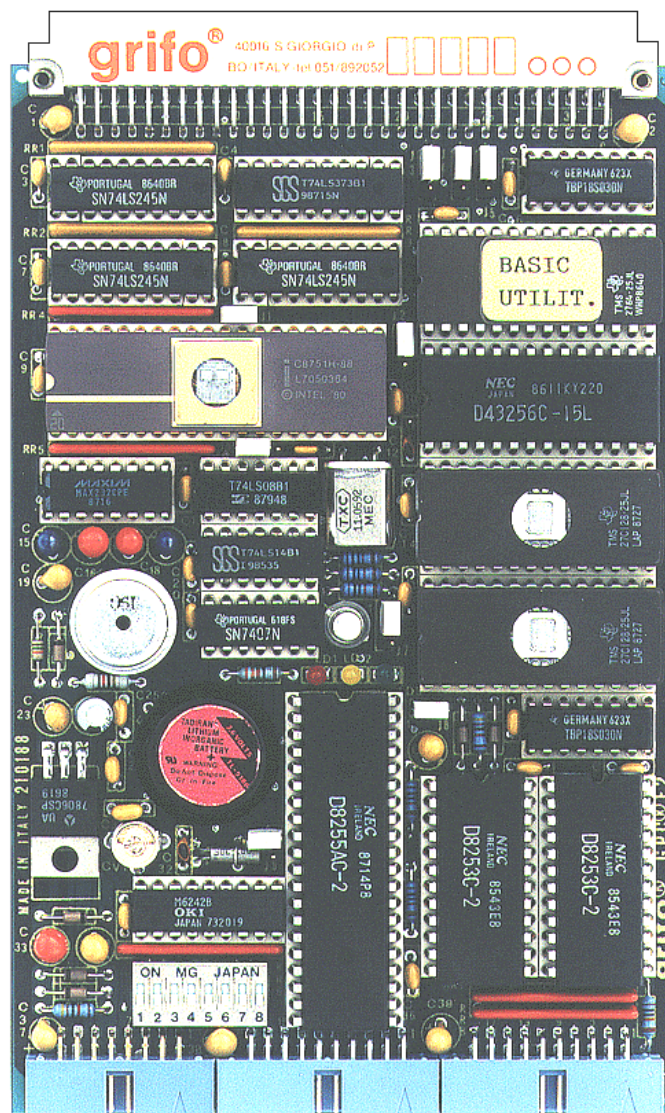


# GPC<sup>®</sup> F2

General Purpose Controller 51 Family

## TECHNICAL MANUAL



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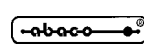
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GPC<sup>®</sup> F2

Edition 3.00

Rel. 18 January 1999

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# GPC<sup>®</sup> F2

## General Purpose Controller 51 Family

### TECHNICAL MANUAL

Europe size card 100x160 mm for **ABACO<sup>®</sup>** BUS. **80Cxxx** CPUs with clock from **11** to **22** MHz (80C32, 87C52, 80C320, etc). Sockets up to max **96K** of memory divided in: 32K RAM,EPROM; 32K RAM,EEPROM; 16+16K programmable EPROMs. **Programming** socket for two EPROMs also with intelligent algorithm. **16** digital **I/O** lines, managed by software. 8 ways **dip switch** readable from software; if necessary it can be changed in others **8** I/O digital lines. **3 LEDs** for feedback of the different card statuses. On board **buzzer** for sound, driven by a **PWM** line available on connector. Up to **three 16 bit timers counters** with related control lines, inside the CPU. **Six** 16 bit timers counters, driven by **82C54**, capable of frequency and counting signals management. **2 RS 232** serial line, one full duplex and the other half duplex. Connector interface for 8 bit BUS **ABACO<sup>®</sup>**. Standard I/O **ABACO<sup>®</sup>** connectors with 20 and 16 pins. **Real time clock** calendar that manages date and time by software. **Back up** circuitry for real time clock through on board **lithium** battery. Single power supply **+5 Vdc, 340mA**. Wide range of development software such as: **Monitor; Debugger; Assembler; GET 51** and **BASIC Interpreter; BASIC, PASCAL** and **C compilers; FORTH; PLM 51**; etc.

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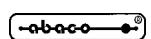
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### IMPORTANT

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**grifo®** reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

### SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

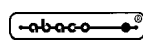


Attention: Generic danger



Attention: High voltage

### Trade marks

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Other Product and Company names listed, are trade marks of their respective companies.

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## INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

## CARD VERSION

The present handbook is reported to the GPC® F2 card release **130688** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example in the left low corner of the component side).

## GENERAL FEATURES

The **GPC® F2** is a powerful control module of **ABACO®** family, capable of operating in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or acquisition network, with an excellent price/performance ratio.

The extreme modularity of this card makes the same the ideal component for the construction of architectures with distributed logic affording good resources both in terms of processing and I/O interconnections. The completeness of **GPC® F2** makes it suitable to meet on its own, control requirements of medium complex units or automations. When a more complex system is required, the performances are increased using suitable **grifo®** cards to be assembled on the powerful industrial **ABACO®** BUS. Each connector has standard pins out that allows a direct connection with all the **I/O BLOCK** module or a fast and inexpensive connection with proper field interface manufactured by the user and other companies.

The most interesting characteristic of **GPC® F2** is that it can be equipped with a wide range of  $\mu$ P. It is in fact possible to get it by the standard **80C32**; by the fast **DALLAS 80C320** and many of the compatible models, either with or without internal ROM. The characteristics of the card remain basically the same, but its performance changes according to the built in  $\mu$ P.

At present there are some developing software tools which allow the card to be used as developing system of itself both in assembler and evolved languages. Noteworthy among these are the development tools as the **C compilers**, the **BASCOM 8051** and the handy **BASIC F2**. With these software tools the user can develop its application programs in a very fast and comfortable environment; it is sufficient a serial connection to a common personal computer.

- Europe size card 100x160 mm for **ABACO®** BUS.
- **80Cxxx** CPUs with clock from **11** to **22** MHz (80C32, 87C52, 80C320, etc).
- Sockets up to max **96K** of memory divided in: 32K RAM, EPROM; 32K RAM, EEPROM; 16+16K programmable EPROMs.
- **Programming** socket for two EPROMs also with intelligent algorithm.
- **16** digital I/O lines, managed by software.
- 8 ways **dip switch** readable from software; if necessary it can be changed in others **8** I/O digital lines.
- **3 LEDs** for feedback of the different card statuses.
- On board **buzzer** for sound, driven by a **PWM** line available on connector.
- Up to **three 16 bit timers counters** with related control lines, inside the CPU.
- **Six** 16 bit timers counters, driven by **82C54**, capable of frequency and counting signals management.
- **2 RS 232** serial line, one full duplex and the other half duplex.
- Connector interface for 8 bit BUS **ABACO®**.
- Standard I/O **ABACO®** connectors with 20 and 16 pins.
- **Real time clock** calendar that manages date and time by software.
- **Back up** circuitry for real time clock through on board **lithium** battery.
- Single power supply **+5 Vdc, 340mA**.
- Wide range of development software such as: **Monitor; Debugger; Assembler; GET 51** and **BASIC Interpreter; BASIC, PASCAL** and **C compilers; FORTH; PLM 51**; etc.

The following pages describe each section of the card in a more detailed mode and figure 1 illustrates the sections interconnections.

## CPU

The **GPC® F2** can use many of '51 microprocessors family as 80C32, 80C52, 87C52 89C52, etc. (from INTEL and other second sources), 80C320, 87C320 (manufactured by DALLAS). These 8 bit microprocessors are code compatible with the world wide used 8051 INTEL and they have an extended instruction set, fast execution time, easy use of all kind of memory and an efficient interrupt management. The most important features of the described microprocessor, are:

- μP 80C32:**
- 8 bit CPU;
  - 12 clocks system cycle;
  - 256 bytes internal RAM;
  - 8K bytes internal ROM;
  - 64K + 64K bytes of external code and data memory;
  - four 8 bits I/O port;
  - 2 standard 16 bits Timer/Counters;
  - 16 bits Timer/Counters with Capture and Compare function;
  - 2 priority level for interrupts and 6 interrupt sources;
  - 1 synchronous/asynchronous serial line;
  - Idle mode or Power down mode;
- μP 80C320:**
- 8 bit CPU;
  - 4 clocks system cycle;
  - 256 bytes internal RAM;
  - 8K bytes internal ROM;
  - 64K + 64K bytes of external code and data memory;
  - four 8 bits I/O port;
  - 2 standard 16 bits Timer/Counters;
  - 16 bits Timer/Counters with Capture and Compare function;
  - 3 priority level for interrupts and 13 interrupt sources;
  - 2 synchronous/asynchronous serial line;
  - power failure section;
  - internal watch dog timer;
  - Idle mode or Power down mode;

For further information, please refer to specific documentation of the manufacturing company.

## BUS ABACO®

One of the most important features of **GPC® F2** is its possibility to be interfaced to industrial **ABACO® BUS**: a standard connector that allows card connection to some of the numerous **grifo®** boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition (A/D), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc.

Using **ABB 03** or **ABB 05** mother boards it is possible manage all the **ABACO®** I/O BUS peripheral card in 3 and 4 type. So **GPC® F2** becomes the right component for many industrial automation systems, in fact it is easily expandable, with the best price/performance ratio.

## CLOCK DEVICE

On **GPC® F2** there are two separate circuits with crystal to generate the clock signal for the microprocessor (from 11.0592 to 22.1184 MHz) and the clock signal for the real time clock (32.768 KHz). The choice of using two circuits and two separated crystals, has the advantage to change the microprocessor working speed (when best performances are required) without additional changes in software, firmware, etc. Please remember that the microprocessor clock frequency indirectly defines the baud rate of the serial line and that this frequency must be specified at the moment of the order, as if not specified, the default value is 11.0592 MHz.

## PERIPHERAL DEVICES

**GPC® F2** is the right card to solve many control problems in automation fields, in fact it is equipped with some peripheral components that facilitate the connection and the management to external system. These peripherals are:

- **Real time clock:** this device includes a clock calendar capable to self manage day, month, year, hours, minutes, seconds, and day of the week. These data can be read and setted by software through 16 registers allocated in CPU addressing space. The component is backed with lithium battery.
- **Buzzer:** it is a circuit based on a capacitive buzzer that emits a wide range of sound, programmed by software. This circuit is driven by a PWM signals driven by CPU and it can be used to manage alarm, sound feed back, etc.
- **PPI 82C55:** it manages 24 TTL digital I/O lines divided in three 8 bit parallel ports. The lines can be used to expand the card use (i.e. management of not intelligent peripheral, interface, etc.) and their direction is software settable at byte level. The PPI 82C55 is completely driven by software programming the 4 registers allocated in the addressing space of the microprocessor.
- **Two PT 82C54:** these devices includes six 16 bits timers counters that are programmable by software, modular and independent. Thanks to a simple external circuit it is really easy to use the 82C54 to acquire encoders or to generates analog signals. With this inexpensive addition the **GPC® F2** becomes a powerfull two axis control system. The software management of these devices is based on 8 registers allocated in CPU addressing space, by the card control logic.
- **Card configuration:** on the board is available a dip switch with 8 dips connected to PPI 82C55 port B and some jumpers, that can be acquired by software. These configuration inputs are normally used to configure the card and its application software. Moreover some status LEDs are also available on **GPC® F2** and they can be used to shows the system status.

For further information about peripheral devices please refer to the technical documentation of the manufacturing company.

## CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on **GPC® F2** are assigned from a specific control logic that allocates all these devices in the microprocessor addressing space. For further information please refer to chapter "ADDRESSES AND MAPS" of this manual.

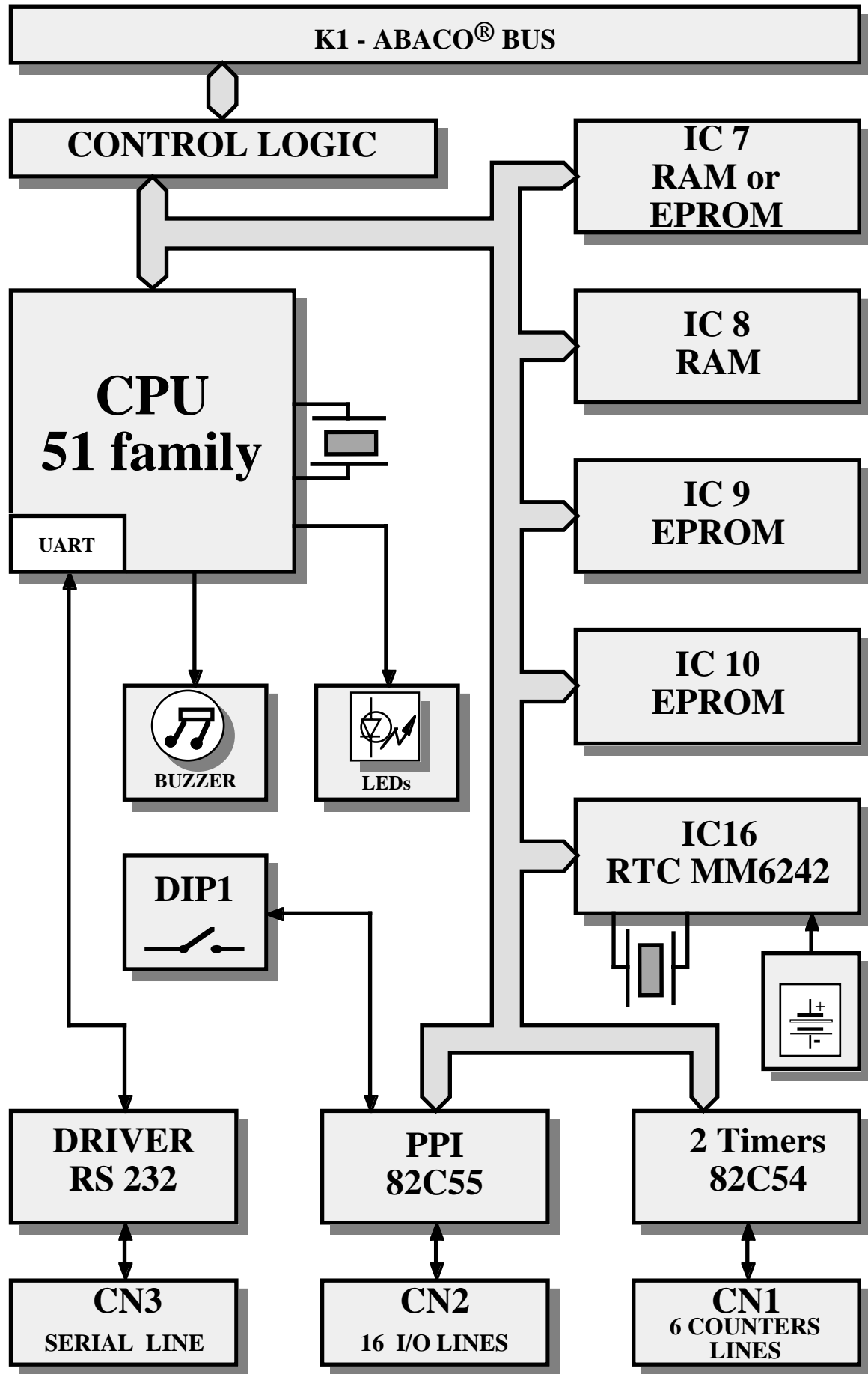


FIGURE 1: BLOCK DIAGRAM

## MEMORY DEVICES

On the card can be mounted 96K of memory divided with a maximum of **32K** EPROM, RAM; **32K** RAM, EEPROM; and **32K** of programmable EEPROM. The **GPC® F2** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 32K byte of static RAM and all different configurations must be specified from the user, at the moment of the order. By mounting backed RAM module or EEPROM module, there is the possibility to keep data also when power supply is missed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The addressing of memory devices is controlled by a specific control logic, that provides to allocate the devices in the microprocessor address space, this control logic automatically manages the different addressing mode and it satisfy the requests of each **GPC® F2** software tools.

For further information about memory configuration, sockets description and jumpers connection, please refer to "ADDRESSES AND MAPS" chapter and to "MEMORY SELECTION" paragraph.

## SERIAL COMMUNICATION

An hardware serial line is always available on **GPC® F2** (named primary serial) and it is completely software configurable for physical protocol (baud rate, stop bits number and lenght of character) by simply programming some microprocessor registers. For further information about primary serial line, please refer to technical documentation of the manufacturing company.

On the card it is also available a second serial line (named auxiliary serial) that is driven by a microcontroller I/O line and it is half duplex. For this software serial line the physical protocol is completely defined by the software procedures. Some software tools (**BASIC F2**, etc.) directly manages the auxiliary lines through high level instructions.

Both primary and auxiliary serial lines are always RS 232 buffered.

## RESET CONTACT

On **GPC® F2** there is a comfortable reset contact that allows the activation of card reset circuit. By connecting J8, the card restarts execution of the program saved in EPROM and all the on board peripheral devices are reset at the same time. J8 is commonly used to exit from endless loop, especially during debug phase and if it is necessary it can be connected to a normally open button mounted far from the card.

## TECHNICAL FEATURES

### GENERAL FEATURES

<b>Devices:</b> (without $\mu$ P resources)	<ul style="list-style-type: none"> <li>24 programmable TTL input/output lines</li> <li>1 bidirectional RS 232 serial line (primary)</li> <li>1 monodirectional RS 232 serial line (auxiliary)</li> <li>1 local contact for reset</li> <li>1 Real time clock</li> <li>3 status LEDs</li> <li>1 octal dip switch</li> <li>1 <b>ABACO® BUS</b> expansion interface</li> <li>1 buzzer</li> <li>6 timer counter with 16 bits</li> </ul>
<b>Memory:</b>	<ul style="list-style-type: none"> <li>IC 7: From 8K x 8 to 32K x 8 EPROM 8K x 8 RAM</li> <li>IC 8: from 8K x 8 to 32K x 8 RAM 32K x 8 EEPROM</li> <li>IC 9: from 8K x 8 to 16K x 8 EPROM</li> <li>IC 10: from 8K x 8 to 16K x 8 EPROM</li> </ul>
<b>BUS features:</b>	8 data bits; 16 addresses bits
<b>CPU:</b>	INTEL 80C32 and compatible ones. DALLAS 80C320 and compatible ones.
<b>Clock frequency:</b>	<ul style="list-style-type: none"> <li><math>\mu</math>P 80C32: 11.0592 MHz</li> <li><math>\mu</math>P 80C320: 22.1184 MHz</li> </ul>
<b><u>PHYSICAL FEATURES</u></b>	
<b>Size:</b>	100 x 160 x 20 mm (single Euro card)
<b>Weight:</b>	175 g (standard base configuration)
<b>Connectors:</b>	<ul style="list-style-type: none"> <li>K1: 64 pins DIN 41612, male, case C connector</li> <li>CN1: 20 pins, male, 90°, low profile connector</li> <li>CN2: 20 pins, male, 90°, low profile connector</li> <li>CN3: 16 pins, male, 90°, low profile connector</li> </ul>
<b>Temperature range:</b>	0÷70 °C
<b>Relative humidity:</b>	20%÷90% (without condense)

**ELECTRIC FEATURES**

- Power supply voltage:** +5 Vdc
- Consumption on 5 Vdc:** 340 mA (µP 80C32 11.0592 MHz)
- Back up battery:** 3,0 Vdc; 180 mAh
- Back up current:** 2.4 µ A

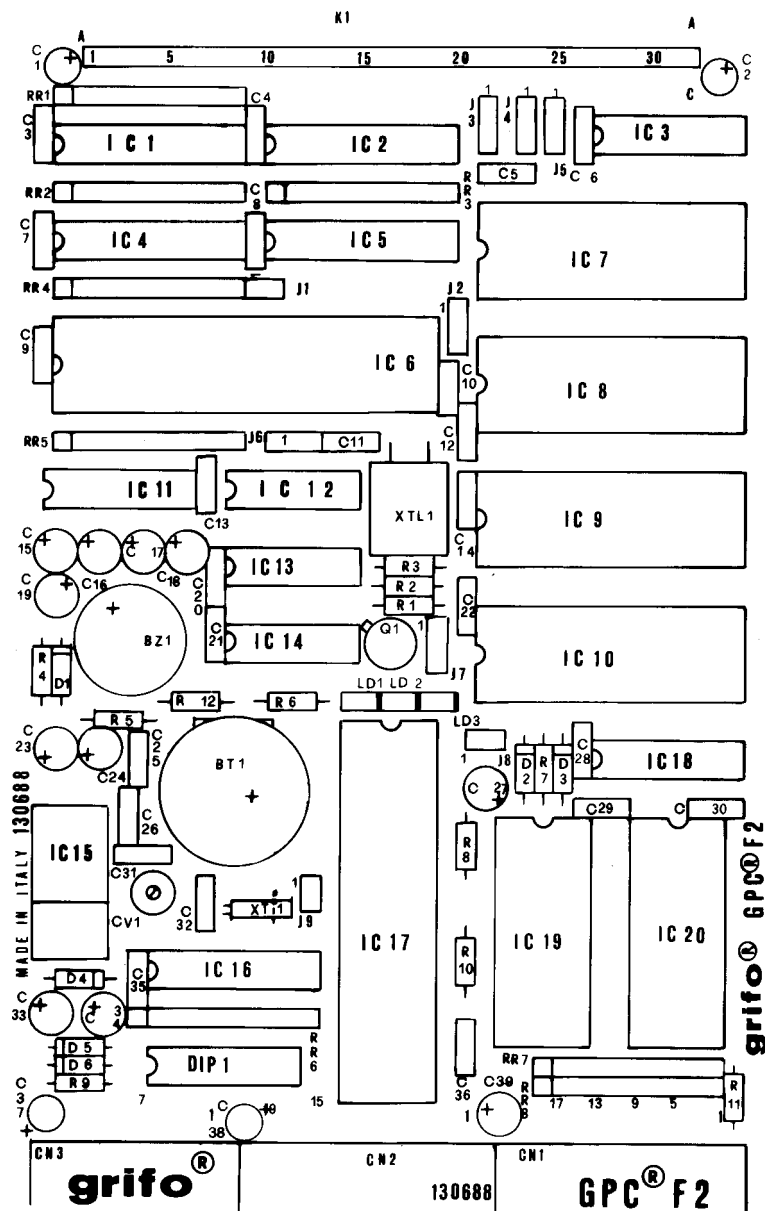


FIGURE 2: COMPONENTS MAP



## INSTALLATION

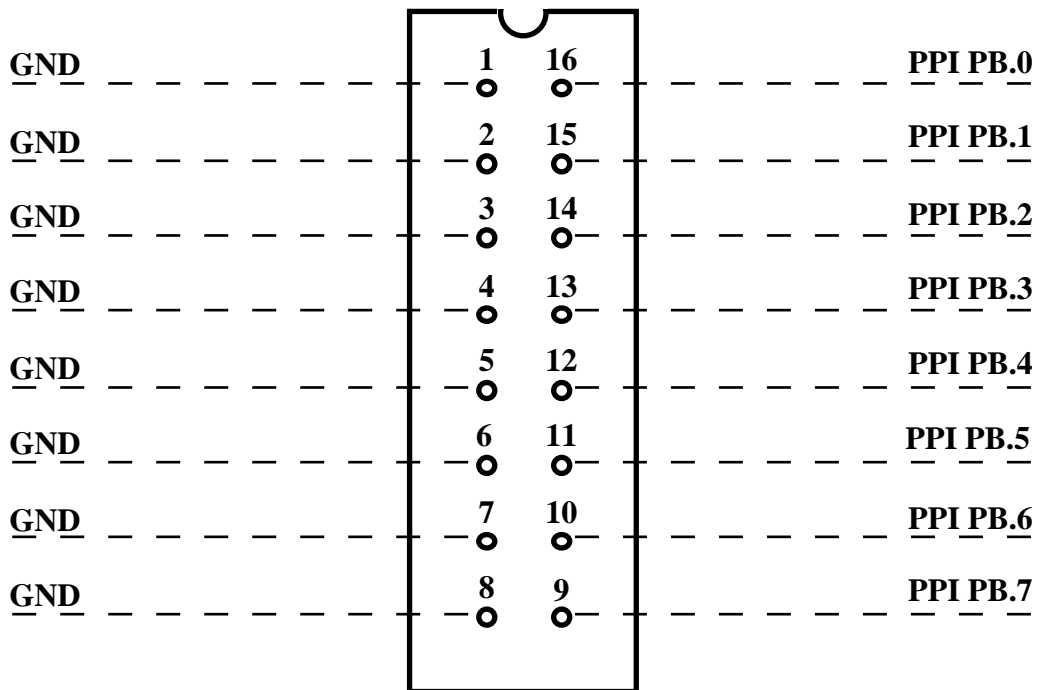
In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers, LEDs and some explanatory diagrams.

### CONNECTIONS

The **GPC®F2** module has 5 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), and connectors location (see figure 12).

#### **DIP 1 - SOCKET FOR PPI 82C55 PORT B**

DIP 1 is a 16 pins socket with 2.54 pitch. By disconnecting the octal dip switch from DIP 1 the PPI 82C55 port B can be used to manage eight TTL digital input output lines. The connection of the obtained 8 I/O lines with external electronics must be performed with proper flat cable DIL connector.



**FIGURE 3: DIP 1 - SOCKET FOR PPI 82C55 PORT B**

Signals description:

- PPI PB.n** = I/O - PPI 82C55 port B digital line n.
- GND** = - Ground signal.

## CN2 - PPI 82C55 PORT A AND C CONNECTOR

CN2 is a 20 pins, male, 90°, low profile connector with 2.54 mm pitch.

On CN2 connector are available PPI 82C55 port A and C equal to 16 I/O digital lines; all these signals follow TTL standard and I/O **ABACO**® standard. CN2 can be used for many purpose as described in the proper chapter "DIGITAL I/O INTERFACE"

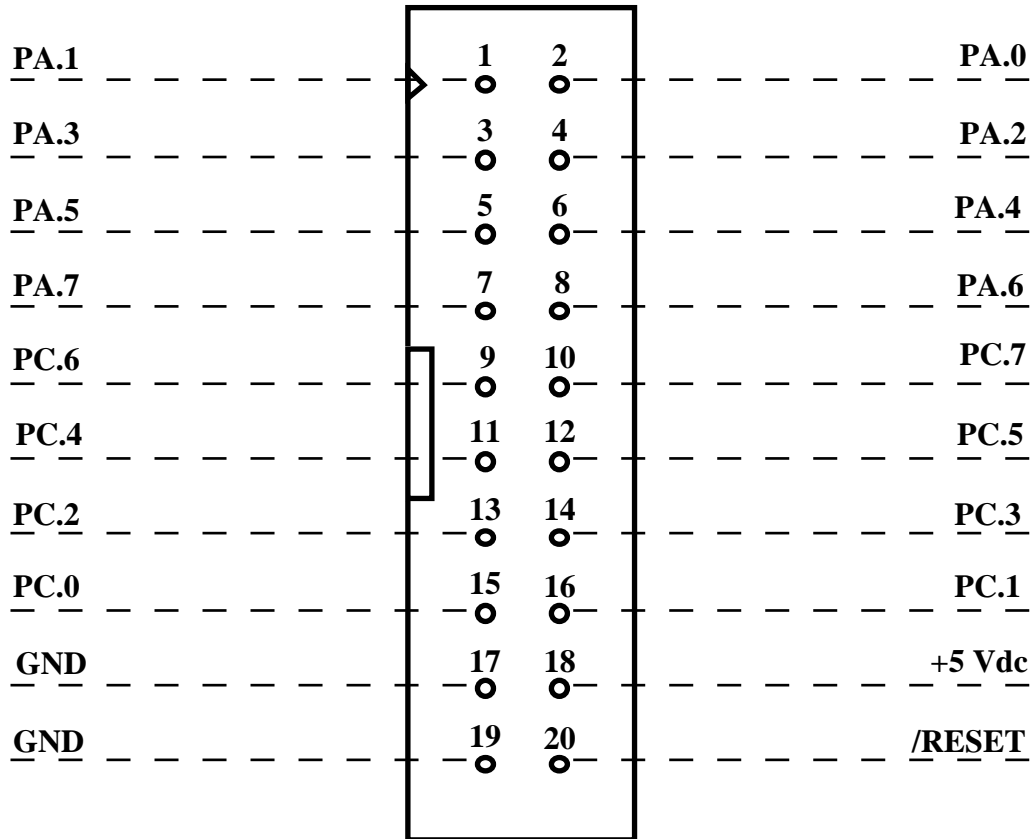


FIGURE 4: CN2 - PPI 82C55 PORT A AND C CONNECTOR

Signals description:

<b>PPI PA.n</b>	=	I/O	- PPI 82C55 port A digital line n.
<b>PPI PC.n</b>	=	I/O	- PPI 82C55 port C digital line n.
<b>/RESET</b>	=	O	- On board reset circuit output signal.
<b>+5 Vdc</b>	=	O	- Line connected to +5 Vdc power supply
<b>GND</b>	=		- Ground signal
<b>N.C.</b>	=		- Not connected

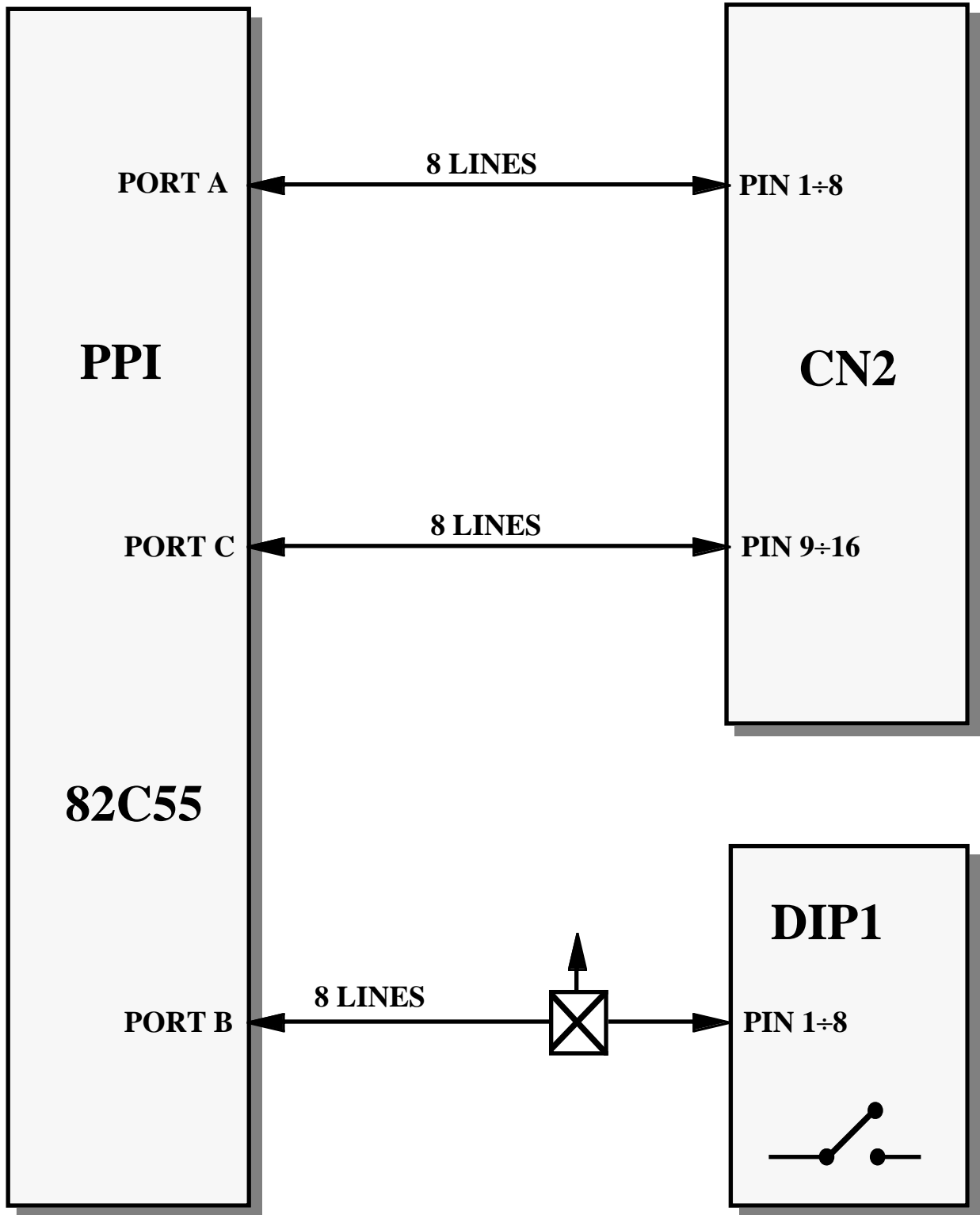


FIGURE 5: CONNECTION DIAGRAM OF PPI 82C55 SIGNALS

### CN3 - SERIAL LINES, TIMER COUNTER, PWM CONNECTOR

CN3 is a 16 pins, male, 90°, low profile connector with 2.54 mm pitch.

On CN3 are reported the two RS 232 serial line signals, the CPU timer counter input and output signals, the CPU PWM signals that drives the on board buzzer and the eventual programming voltage for the EPROM.

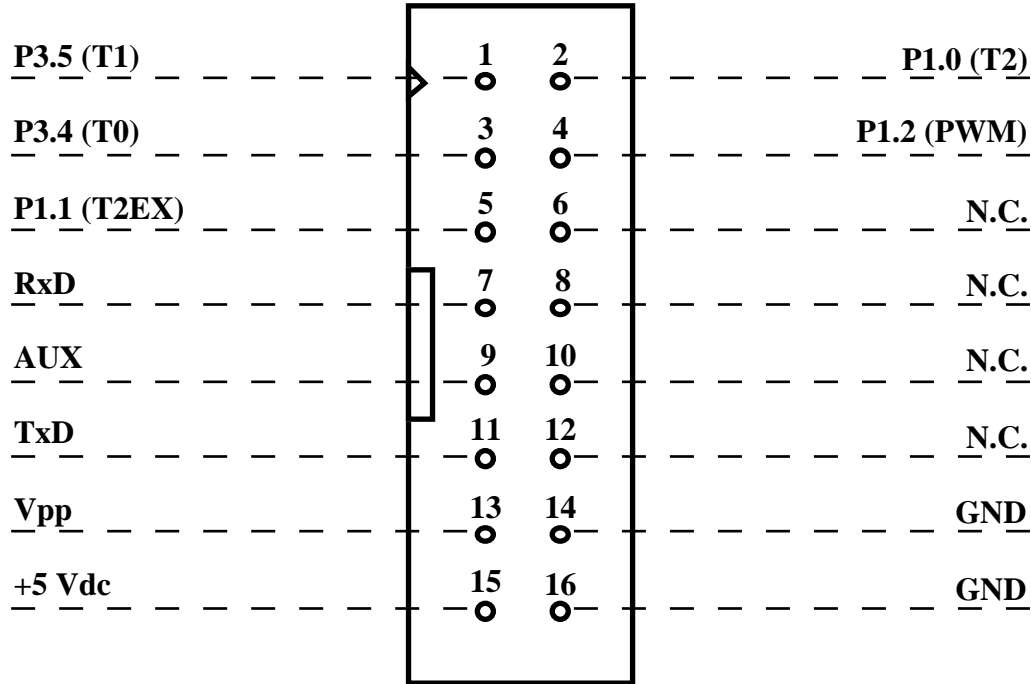


FIGURE 6: CN3 - SERIAL LINES, TIMER COUNTERS, PWM CONNECTOR

Signals description:

<b>Px.y</b>	=	I/O	- CPU digital line y of port x.
<b>Tn</b>	=	I	- Interface signal for CPU timer counter n.
<b>T2EX</b>	=	I	- Capture signal for CPU timer counter 2.
<b>PWM</b>	=	I	- Pulse with modulation signal, driven by CPU through software.
<b>RxD</b>	=	I	- RS 232 receive signal of the primary serial line.
<b>TxD</b>	=	O	- RS 232 transmit signal of the primary serial line.
<b>AUX</b>	=	O	- RS 232 transmit signal of the auxiliary serial line.
<b>Vpp</b>	=	I	- On board EPROM programming voltage, variable from 12.0 to 13.0 Vdc.
<b>+5 Vdc</b>	=	O	- +5 Vdc power supply.
<b>GND</b>	=		- Ground signal.
<b>N.C.</b>	=		- Not connected.

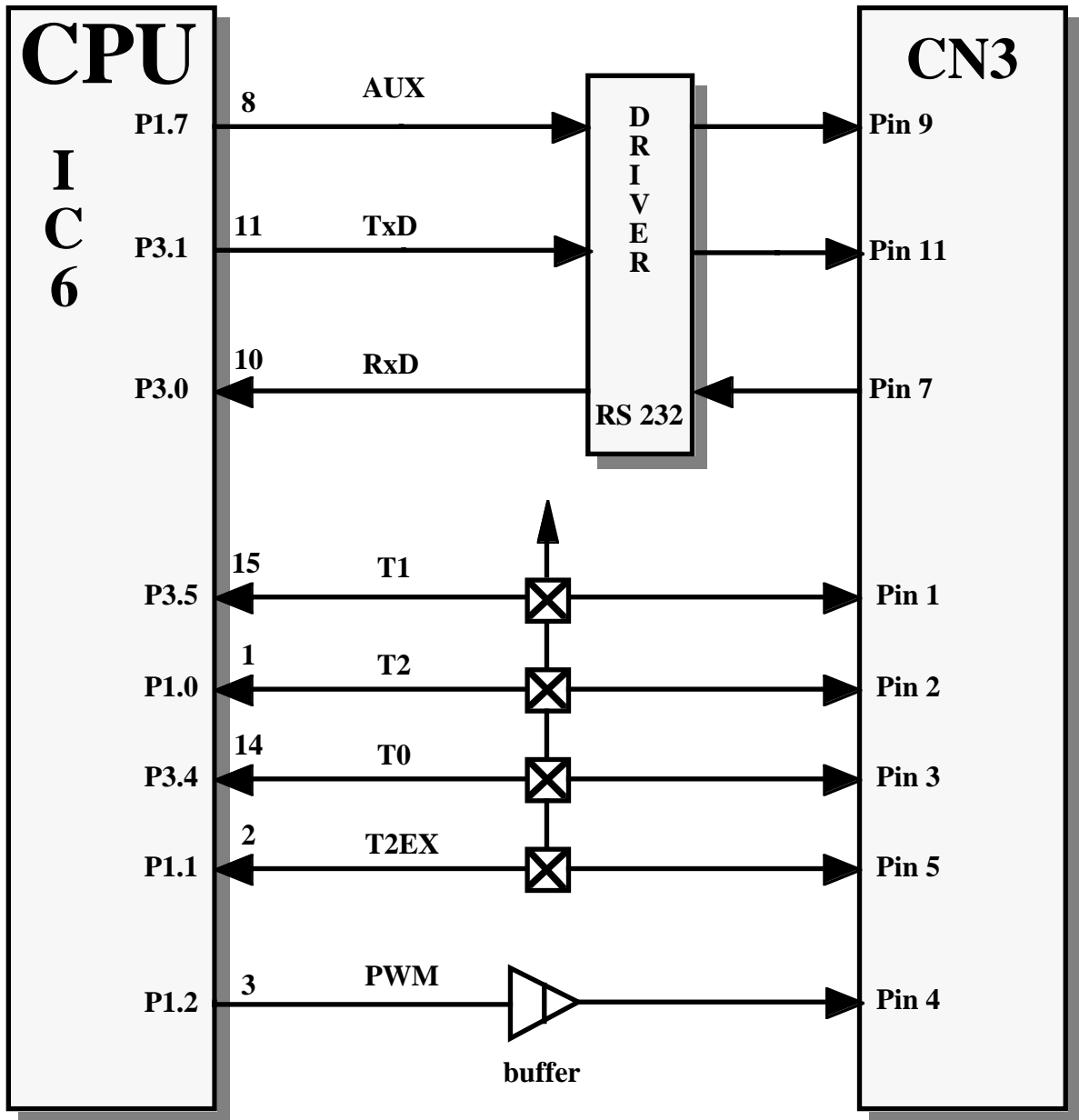


FIGURE 7: CONNECTION DIAGRAM OF CN3 SIGNALS

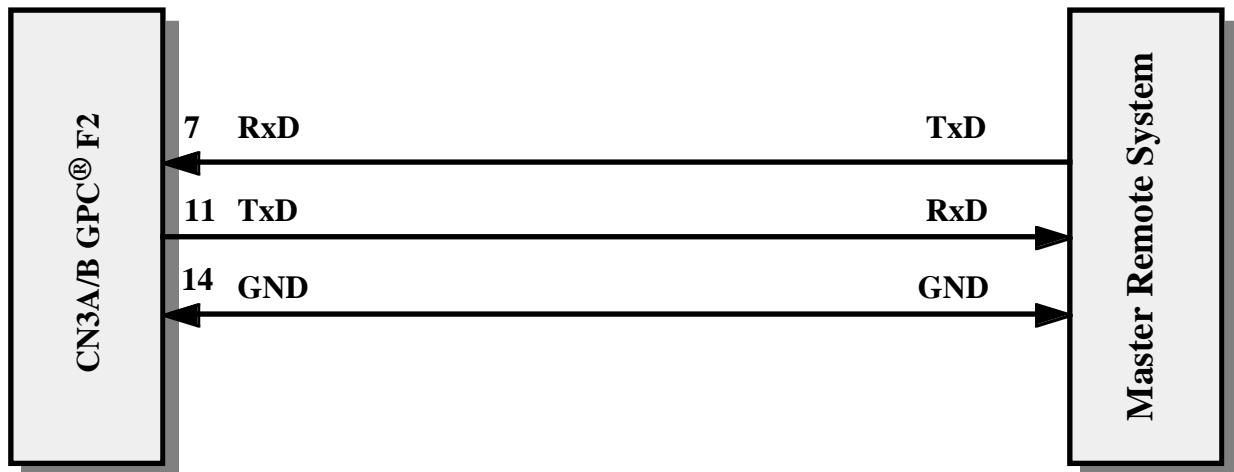


FIGURE 8: RS 232 PIN OUT AND CONNECTION EXAMPLE

## K1 - ABACO® BUS CONNECTOR

K1 is a 64 pins, male, 90°, DIN 41612, case C connector with 2.54 pitch.

On K1 are available all the industrial **ABACO®** BUS signals and it can be used for connections to many other peripheral cards. In the table below there are the standard pin outs both for 8 bits and 16 bits CPU and the signal connected on **GPC® F2**. All signals follow TTL standard.

<b>A</b> <b>BUS a 16 bit</b>	<b>A</b> <b>BUS a 8 bit</b>	<b>A</b> <b>GPC F2</b>	<b>PIN</b>	<b>C</b> <b>GPC F2</b>	<b>C</b> <b>BUS a 8 bit</b>	<b>C</b> <b>BUS a 16 bit</b>
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N.C.		D8
D1	D1	D1	4	N.C.		D9
D2	D2	D2	5	N.C.		D10
D3	D3	D3	6	/INT	/INT	/INT
D4	D4	D4	7	/NMI	/NMI	/NMI
D5	D5	D5	8	N.C.	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	N.C.	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	N.C.	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	N.C.	/M1	/IACK
A7	A7	A7	18	N.C.	/RFSH	D14
A8	A8	A8	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	A9	20	N.C.	VDUSEL	A22
A10	A10	A10	21	N.C.	/IEI	D15
A11	A11	A11	22	N.C.		
A12	A12	A12	23	N.C.	CLK	CLK
A13	A13	A13	24	N.C.		/RDUDS
A14	A14	A14	25	N.C.		/WRUDS
A15	A15	A15	26	N.C.		A21
A16		N.C.	27	N.C.		A20
A17		N.C.	28	N.C.		A19
A18		N.C.	29	/R.T.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 9: K1 - ABACO® BUS CONNECTOR

## Signals description:

## 8 bits CPU

<b>A0÷A15</b>	=	O	- Address BUS
<b>D0÷D7</b>	=	I/O	- Data BUS
<b>/INT</b>	=	I	- Interrupt request
<b>/NMI</b>	=	I	- Non Maskable Interrupt
<b>/HALT</b>	=	O	- Halt state
<b>/MREQ</b>	=	O	- Memory Request
<b>/IORQ</b>	=	O	- Input Output Request
<b>/RD</b>	=	O	- Read cycle status
<b>/WR</b>	=	O	- Write cycle status
<b>/BUSAK</b>	=	O	- BUS Acknowledge
<b>/WAIT</b>	=	I	- Wait
<b>/BUSRQ</b>	=	I	- BUS Request
<b>/RESET</b>	=	O	- Reset
<b>/M1</b>	=	O	- Machine cycle one
<b>/RFSH</b>	=	O	- Refresh for dynamic RAM
<b>/MEMDIS</b>	=	I	- Memory Display
<b>VDUSEL</b>	=	O	- VDU Selection
<b>/IEI</b>	=	I	- Interrupt Enable Input
<b>CLK</b>	=	O	- System clock
<b>R.B.</b>	=	I	- Reset button
<b>+5 Vdc</b>	=	I	- Power supply at +5 Vdc
<b>+12 Vdc</b>	=	I	- Power supply at +12 Vdc
<b>-12 Vdc</b>	=	I	- Power supply at -12 Vdc
<b>GND</b>	=		- Ground signal

## 16 bits CPU

<b>A16÷A22</b>	=	O	- Address BUS
<b>D8÷D15</b>	=	I/O	- Data BUS
<b>/RD UDS</b>	=	O	- Read Upper Data Strobe
<b>/WR UDS</b>	=	O	- Write Upper Data Strobe
<b>/IACK</b>	=	O	- Interrupt Acknowledge
<b>/RD LDS</b>	=	O	- Read Lower Data Strobe
<b>/WR LDS</b>	=	O	- Write Lower Data Strobe

## Note:

The signals directions used in the upper description refer to a control or command card (**CPU** or **GPC**®) and they are not changed neither on peripheral card, to avoid ambiguous indications when system with more than one cards are realized.

## CN1 - PT 82C54 CONNECTOR

CN1 is a 20 pins, male, 90°, low profile connector with 2.54 mm pitch.

On CN1 are available the 6 timers counters signals of the two on board PT 82C54. Through this connector the **EMI 01** card can be directly connected, obtaining a low cost axis control system. All the signals are at TTL level and they are placed in order to reduce interference and electrical noise.

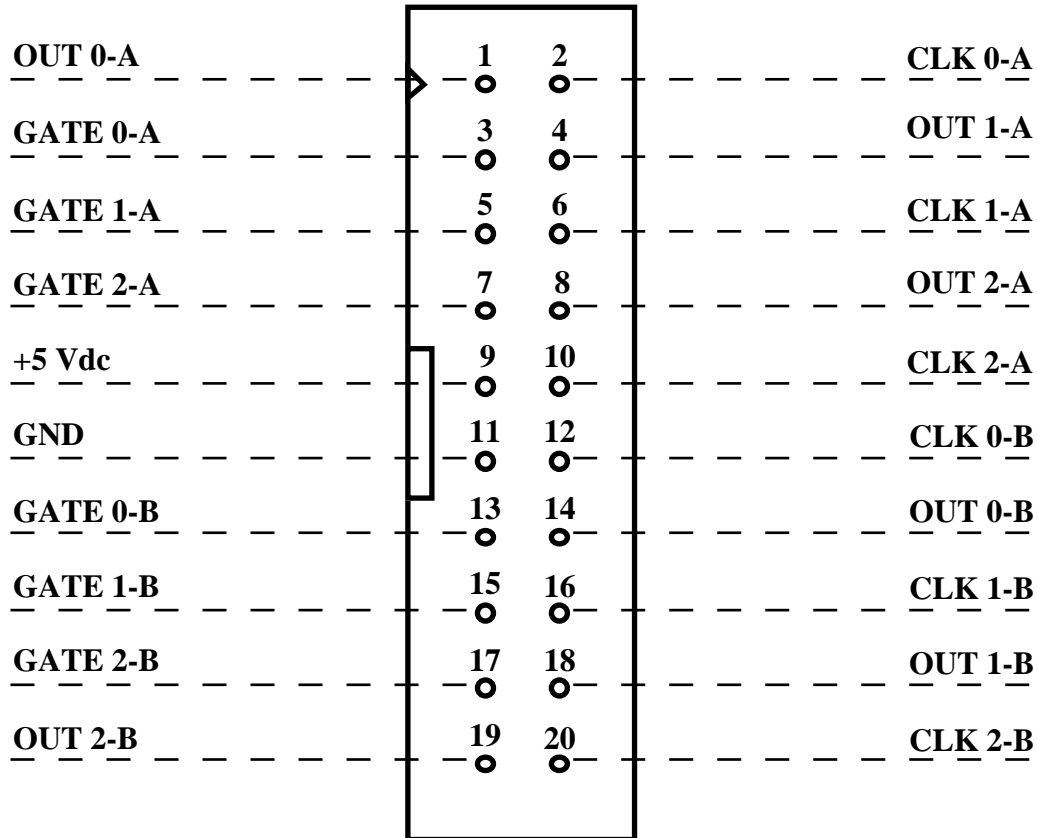


FIGURE 10: CN1 - PT 82C54 CONNECTOR

Signals description:

<b>OUT x-y</b>	=	O	- Output signal for timer counter x of PT 82C54 y.
<b>GATE x-y</b>	=	I	- Trigger signal for timer counter x of PT 82C54 y.
<b>CLK x-y</b>	=	I	- Clock signal for timer counter x of PT 82C54 y.
<b>+5 Vdc</b>	=	O	- +5 Vdc power supply.
<b>GND</b>	=		- Ground signal.

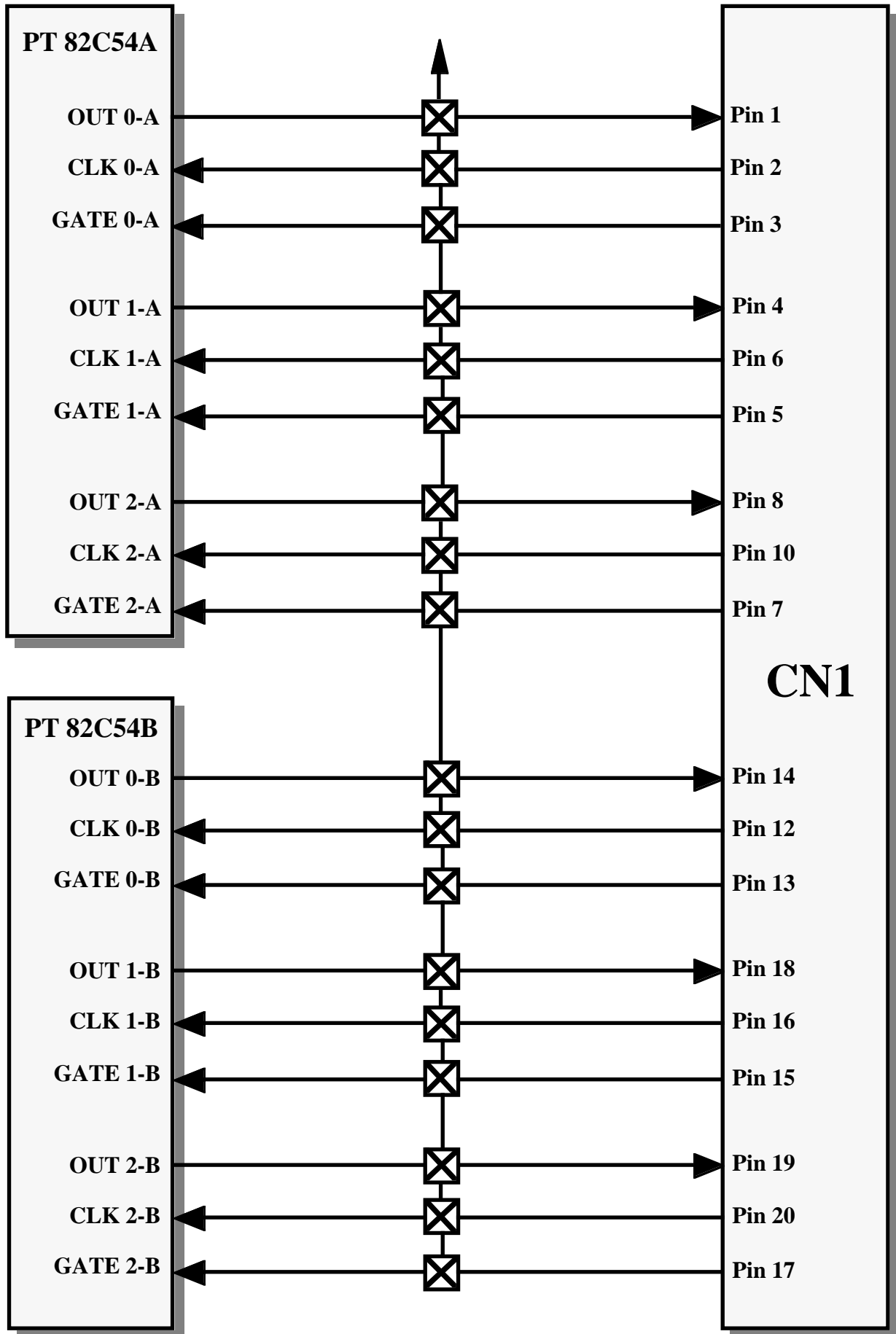


FIGURE 11: CONNECTION DIAGRAM OF PT 82C54 SIGNALS

## DIGITAL I/O INTERFACES

With CN2 (standard I/O ABACO® connector) the GPC® F2 can be connected to some of the numerous grifo® boards modules that have the same pin out. The connection of all these external modules is really simple in fact only a 20 ways flat cable (order code FLT.20+20) is necessary, that connects the power supply too. About software the use of digital I/O interfaces is likewise easy in fact GPC® F2 software tools include proper drivers, library, example, etc.

Below there is a brief description of the supported interfaces:

- **QTP 16P, QTP 24P, KDx x24, DEB 01**, etc.: they are useful local operator panels. These boards already have all the resources (alphanumeric displays, matrix keyboards, LEDs etc) necessary to solve the common man machine communication problems at a short distance from GPC® F2. For software the programmer can use the relative procedure contained in all the GPC® F2 software tools. These procedures normally are drivers software added to the language and they use directly its console instructions (for example INPUT and PRINT for BASIC, PRINTF and SCANF for C etc. ), so for the user is very simple to write on displays and to get data from keyboards.
- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards (RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system that allows read and write of data through the high level files instructions, of the selected programming language.
- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (PRINT for BASIC, PRINTF for C, WRITE for PASCAL, etc.).
- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For further information about the digital I/O interfaces please read "EXTERNAL CARD" chapter and the software tools documentation.

## I/O CONNECTION

To prevent possible connecting problems between GPC® F2 and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232 communication signals the user must follow the standard rules of this protocol.
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground and if an electric insulation is necessary, then an opto coupled interface must be connected. For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corrisponds to logic state "1".

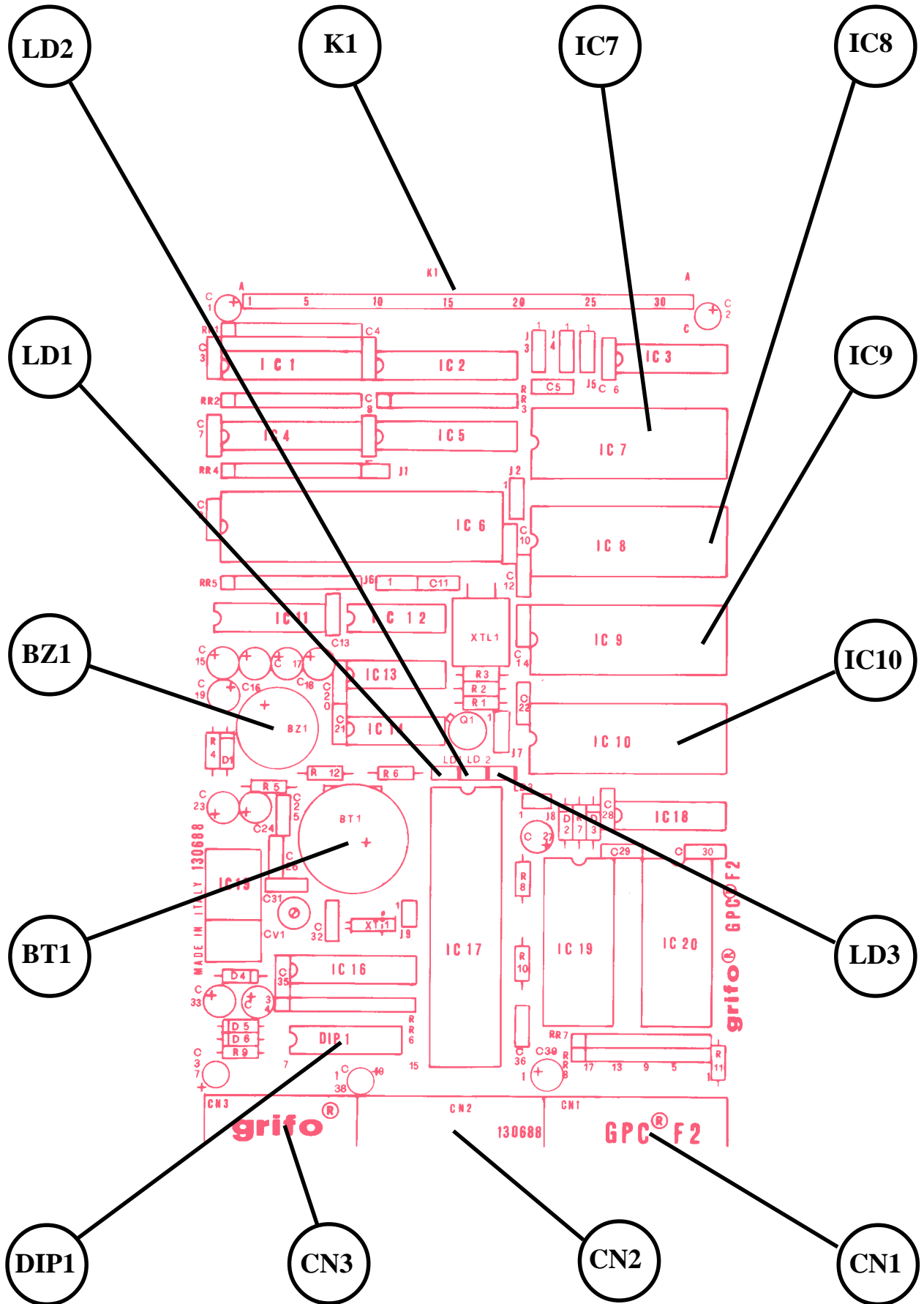


FIGURE 12: LEDs, CONNECTORS, DIP SWITCH, MEMORY, ETC. LOCATION



## LEDS

On **GPC® F2** there are 3 LEDs that shows some card status, as described in the following table:

LED	COLOR	FUNCTION
LD1	Yellow	It indicates, when enabled, the 0 logic status of CPU P1.2 (PWM) signal. In this way the buzzer activation is displayed, also when subsound are generated.
LD2	Red	It indicates, when enabled, the 0 logic status of CPU P1.5 signal. Please refer to "EPROM BURNING" paragraph.
LD3	Green	It indicates, when enabled, the presence of the programming voltage on pin 13 of CN3. Please refer to "EPROM BURNING" paragraph.

**FIGURE 13: LEDS TABLE**

The main function of LEDs is to inform the user about card status, with a simple visual indication and in addition to this, LEDs make easier the debug and test operations of the complete system. To recognize the LEDs location on the card, please refer to figure 12.

## INTERRUPTS MANAGEMENT

One of the most important **GPC® F2** features is the powerfull interrupts management. Following there is a brief description on interrupt hardware signals management of the card:

- /INT **ABACO®** BUS (K1) -> generates an interrupt signal on pin 13 (/INT1) of CPU if J6 is connected in 1-2 position;
- /NMI **ABACO®** BUS (K1) -> generates an interrupt signal on pin 12 (/INT0) of CPU.

Moreover all the CPU internal peripheral devices (timer counters, serial, etc.) can generate interrupts requests. For further information about all internal interrupts and the interrupt mangement by the CPU, please refer to specific documentation of the manufacturing company.

## POWER SUPPLY

The card must be powered only with +5 Vdc. As described in previous paragraphs, the two power supply signals (+5 Vdc and GND) are available on all the card connectors, but to minimize the lay out problems the power should be supplied from **ABACO®** BUS connector (K1), connecting all the proper 8 pins (1, 2, 31, 32 A and C).

If this rule complicates the card installation, the user can supply the power through the others connectors, but only after a carefull test and check.

## JUMPERS

On **GPC® F2** there are 9 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Here below is the jumpers list, location and function:

NAME	PIN N°	FUNCTION
J1	2	Selects CPU internal ROM activation.
J2	3	Selects IC8 RAM size.
J3	3	Selects IC7 memory devices type.
J4	3	Selects memories maps.
J5	3	Selects memories maps.
J6	3	Selects CPU P3.3 (/INT1) signal connection.
J7	3	Selects IC9 and IC10 power supply voltage.
J8	2	Reset contact.
J9	2	Selects on board battery connection.

**FIGURE 14: JUMPERS SUMMARIZING TABLE**

The following tables describe all the right connections of **GPC® F2** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 17.

The "\*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

## 2 PINS JUMPERS

JUMPER	CONNECTION	USE	DEF.
J1	not connected	Enables the eventual internal ROM of the CPU.	*
	connected	Disables the eventual internal ROM of the CPU.	
J8	not connected	Disables reset circuit.	*
	connected	Enables reset circuit.	
J9	not connected	Back up battery non connected to real time clock.	*
	connected	Back up battery connected to real time clock.	

FIGURE 15: 2 PINS JUMPERS TABLE

## 3 PINS JUMPERS

JUMPER	CONNECTION	USE	DEF.
J2	1-2	Configures IC8 for 8K RAM.	*
	2-3	Configures IC8 for 32K RAM, EPROM.	
J3	1-2	Configures IC7 for 8K RAM or 8 and 16K EPROM.	*
	2-3	Configures IC7 for 32K EPROM.	
J4	1-2	Selects IC8 memory device addresses. Please refer to "MEMORY MAPS" paragraph.	*
	2-3		
J5	1-2	Selects IC7 memory device addresses7. Please refer to "MEMORY MAPS" paragraph.	*
	2-3		
J6	1-2	Connects CPU P3.3 (/INT1) signal to /INT1 signal on K1.	*
	2-3	Connects CPU P3.3 (/INT1) signal to GND.	
J7	1-2	Selects a +5 Vdc power supply voltage for IC9 and IC10 EPROM.	*
	2-3	Selects a +6 Vdc power supply voltage for IC9 and IC10 EPROM.	

FIGURE 16: 3 PINS JUMPERS TABLE

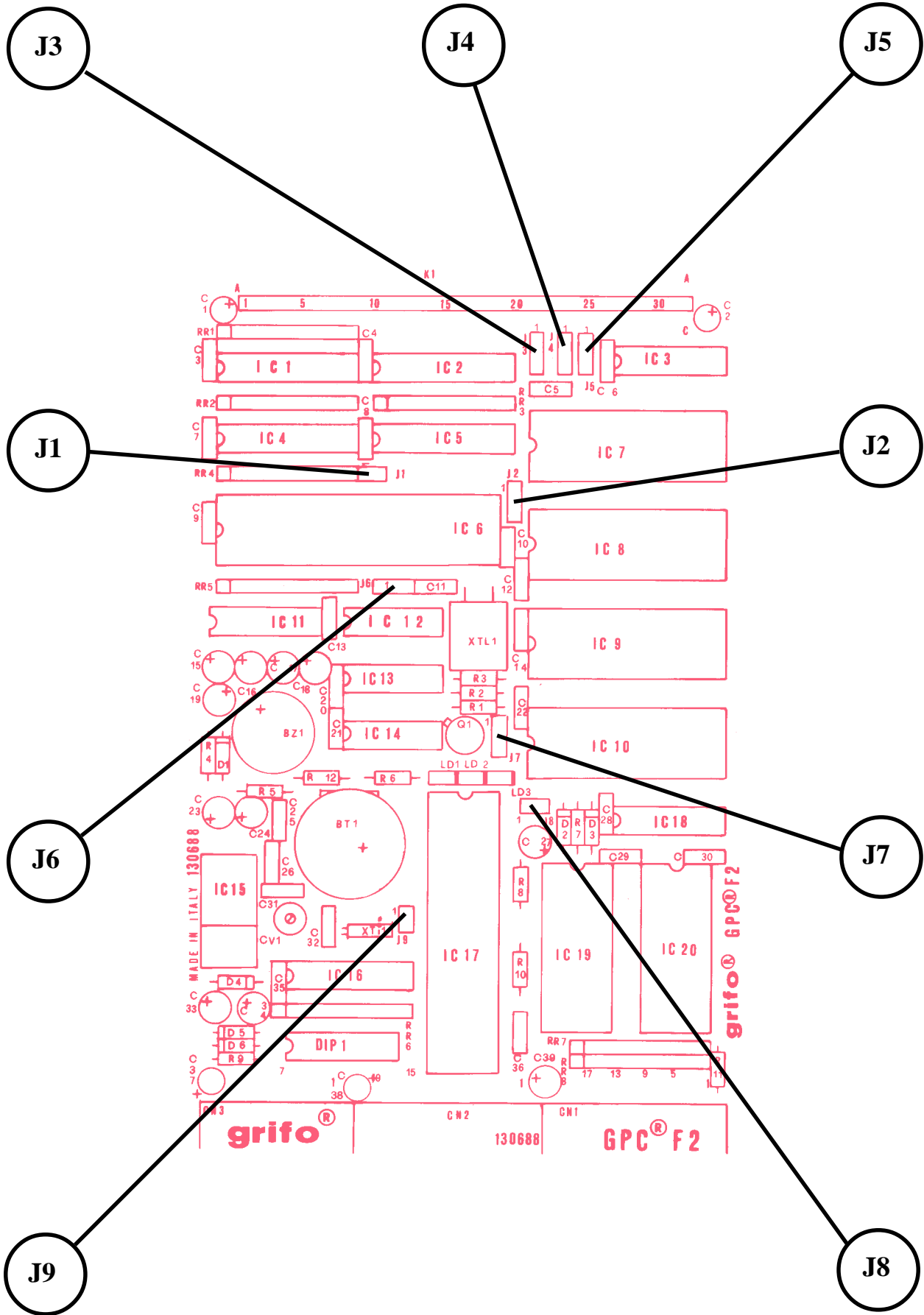


FIGURE 17: JUMPERS LOCATION



## MEMORY SELECTION

On **GPC® F2** can be mounted 96K bytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	JUMPER CONFIGURATION
7	EPROM	8K Bytes	J3 in position 1-2
	EPROM	16K Bytes	J3 in position 1-2
	EPROM	32K Bytes	J3 in position 2-3
	RAM, backed RAM	8K Bytes	J3 in position 1-2
8	RAM, backed RAM	8K Bytes	J2 in position 1-2
	RAM, backed RAM, EEPROM	32K Bytes	J2 in position 2-3
9	EPROM	8K Bytes	-
	EPROM	16K Bytes	-
10	EPROM	8K Bytes	-
	EPROM	16K Bytes	-

FIGURE 18: MEMORY SELECTION TABLE

All the sockets follow the JEDEC standard, so the mounted memory devices must have JEDEC pin outs. The jumpers configurations described on figure 18 only prearrange the sockets for the indicated memory devices, but there are some other jumpers that set the memory addressing map; for this information, please refer to "MEMORY MAPS" paragraph.

Normally **GPC® F2** is supplied in its default configuration with 32K RAM on IC 8; each different configurations can be defined during order phase or self mounted by the user. Below are reported the abbreviation code of the possible memory options:

.8KMOD	->	8K x 8 backed RAM
.32KMOD	->	32K x 8 backed RAM
.32EE	->	32K x 8 parallel EEPROM

For further information and prices please contact directly **grifo®**.

## EPROM BURNING

On **GPC® F2** is available a comfortable circuit that can burn the IC9 and IC10 EPROMs with user data. This circuit is really interesting especially if used with **BASIC F2** software tools in fact some of the BASIC commands can burn the developed application program directly on the EPROMs. Below are reported some indications for the right use of this circuit:

- 1) The programming voltage for the IC9 and IC10 EPROMs must be connected to to pin 13 of CN3; the value of this voltage must correspond to those required by the used EPROMs in the range 12.0 to 13.0 Vdc. The LD3 LEDs signals the presence of the programming voltage.
- 2) The J7 jumper selects the power supply voltage of the two devices. Please remember that a +6 Vdc power supply enables the intelligent burning which reduces the programming time of each byte. To correctly use this intelligent burning the user must first supply the programming voltage, then connect the J7 jumper in position 2-3 and after start burning; when the burning phase is completed the user must reselect the normal power supply, connecting J7 in position 1-2.

- 3) The CPU P1.5 acts as a /PGM ENABLE signal, or on the other hand it connects the programming voltage (described at point 1) to the pin 1 = Vpp of IC9 and IC10 devices. This signal status is displayed by LD2 LED.
- 4) The CPU P1.4 acts as a /PGM PULSE signal in fact it is connected to pin 27 = /PGM of IC9 and IC10 devices. It must be used to confirm each byte programming cycle.
- 5) The CPU P1.3 acts as a DISABLE signal and when it is set low the A0÷A7 addresses signals are maintained stable. In this way the IC9 and IC10 signals don't change even if the CPU is executing some instructions.
- 6) The burning circuit works correctly if only the relative management code is saved and executed on internal microprocessor ROM.

For further information on burning procedures and high level command use please refer to proper documentation of the software tools.

### **POWER ON AND RESET**

On **GPC® F2** there is a reset and power on circuit that manages the always hard phase of card power up and start. This circuit has the following features:

- Fixed power on time, defined by a proper on board RC circuit;
- reset source from R.B. signal on K1 connector (**ABACO® BUS**);
- reset source from on board J8 contact;
- reset circuit output connected to all the card's section;
- reset circuit output connected to /RESET signal on K1 connector (**ABACO® BUS**);
- reset circuit output connected to /RESET signal on CN2 connector;

As before described the J8 contact can enable the card reset circuit: by connecting the two jumpers pins to a normally open contact (i.e. a button), when the contact is closed (two pins short circuited) the card restarts execution of the program saved in the code area and all the on board peripheral devices are reset at the same time. J8 is commonly used to exit from endless loops especially during debug phase. To recognize J8 location on the board, please refer to figure 17.

### **ON BOARD INPUT**

**GPC® F2** card is equipped with an octal dip switch (DIP1) that can be read by software. It is normally used for system configuration (operating mode selection, card number programming inside a network system, firmware configuration, etc.). Reading the dip switches register by software, the user obtain a negated value (0 -> dip in ON position and 1 -> dip in OFF position) as described in "I/O ADDRESSES" and "PPI 82C55" chapters.

Also the J6 jumper can be used as on board input acquired by software, in fact it is connected to CPU P3.3 that is maintained low if the jumper is in position 2-3 and viceversa maintained high if it is in position 1-2 (award that /INT signal on K1 **ABACO® BUS** connector is not driven by other cards). To recognize J6 and DIP 1 location on the board, please refer to figure 17 and 12.

## SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the user can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the 51 family, can be used.

**MCS BASIC F2:** complete development tools for MCS BASIC (interpreted BASIC language for industrial application). It needs a P.C. for console and program saving operations, while the debug, test and program operations are performed on the card. Special instructions which manage the on board peripheral devices have been added.

**BXC51:** cross compiler for source files written in MCS BASIC F2. It allows a considerable speed increment of the starting MCS BASIC program and it is completely executed on external P.C.

**XPAS51:** cross compiler for PASCAL source program , executable on P.C. with MS-DOS.

**FORTH:** complete software development tools to program the card with FORTH high level language. It needs a P.C. for user interface and it is really interesting for its fast execution and small size, of the generated code.

**MCC 51:** integer cross compiler for source files in standard ANSI C. It produces a source assembly file compatible with MCA 51 or with Intel macro relocatable assembler MCS 51.

**MCA 51:** macro cross assembler available for MS-DOS operating system in absolute and relocatable version. In this relocatable version is supplied with a linker and a library manager.

**MCS 51:** source level debugger and simulator. It is executed on P.C. without any additional hardware and it allows loading of HEX and SYMBOLIC files, breakpoint setting, instruction execution in trace mode, registers and memory dump, etc.

**MCK 51:** it is the sum of MCC 51 and MCA 51 and it is a complete C compiler with an output file type compatible with MCS 51.

**HI TECH C 51:** cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment.

**SYS51CW:** cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, simulator and remote symbolic debugger, included in an easy to use integrated development environment for Windows.

**SYS51PW:** cross compiler for PASCAL source program. It is a powerful software tool that includes editor, PASCAL compiler, assembler, optimizer, linker, library, simulator and remote symbolic debugger, included in an easy to use integrated development environment for Windows.

**MDP:** monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line.

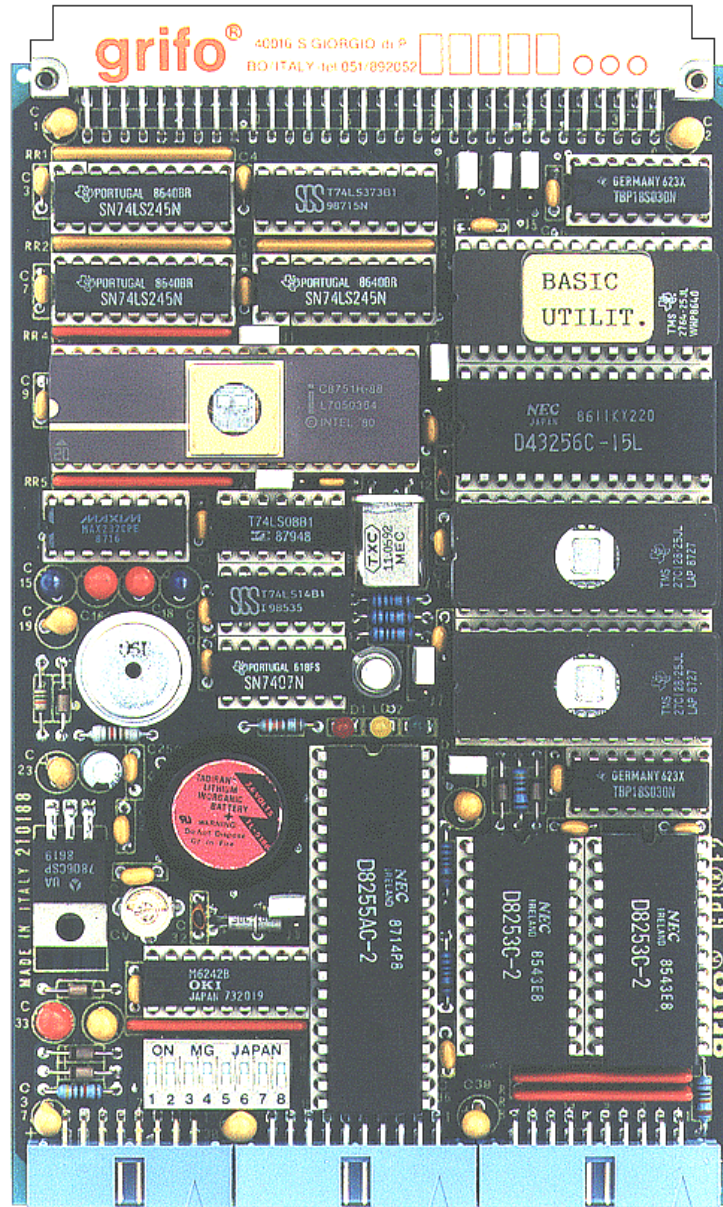


FIGURE 19: CARD PHOTO

**DDS MICRO C 51:** low cost cross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.

**SOFTICE:** It is a remote symbolic debugger with cross assembler. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line. There is an high level user interface that can visualize all the processor status in a multiwindow visualization.

**NOICE:** It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs communicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.

**OPEN 51/UNI:** in circuit emulator for the 51 family. It is a powerful hardware and software tool that includes: source level debugging and symbolic debugging; project management; built-in multi-file editor; execution of external compilers; debugging of several modules at the same time; built-in disassembler; source level step and trace functions; animate functions; inserting and deleting of breakpoints on the source level; watching and modifying variables on symbol and absolute level.

**EMBEDDED PASCAL 51:** cross compiler for PASCAL source program. It is a powerful software tool that includes editor, PASCAL compiler, assembler, optimizer, library, included in an easy to use integrated development environment for Windows 95 and NT. Many memory models and data types are supported and sources of library are provided too.

**BASCOM 8051:** cross compiler for BASIC source program. It is a powerful software tool that includes editor, BASIC compiler and simulator included in an easy to use integrated development environment for Windows. Many memory models, data types and direct use of hardware resource instructions are available.

**GET 51:** it is a complete program with editor, communication driver and mass memory management for all '51 family cards. This program developed by grifo® allows to operate in the best conditions when MCS BASIC, BXC51, MDP software tools are used.

## ADDRESSES AND MAPS

### INTRODUCTION

In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

### ON BOARD RESOURCES ALLOCATION

The card devices addresses are managed by a specific control logic, realized with programmable array logic. This control logic allocates memory and peripheral devices in a comfortable mode for the user. The available microprocessors address 64K bytes of code memory and 64K bytes of data memory and the control logic maps the on board memory and peripheral devices, inside these addresses spaces. Control logic sets size, type and addresses of memory devices through jumpers J2, J3, J4 and J5; at the same time it allocates I/O addresses always in the upper 1.5K bytes of microprocessor memory and it avoids any conflict with the other CPU internal peripheral devices. Summarizing the control logic allocates:

- up to 32K bytes of EPROM, RAM on IC 7;
- up to 32K bytes of RAM, EEPROM on IC 8;
- up to 16K bytes of EPROM on IC 9;
- up to 16K bytes of EPROM on IC 10;
- PPI 82C55;
- two PT 82C54;
- **ABACO®** BUS;
- real time clock;

The addresses of all these devices are described in the following paragraphs and can't be set with different value. The other devices, as status LEDs, buzzer configuration inputs and EPROM burning circuit, are always managed by control logic but they are not allocated in memory space, in fact these device are driven through CPU I/O lines.

### MEMORY MAPS

Actually on **GPC® F2** are available two different control logics for memory maps, named **BU** and **BS**; they are mounted on IC3 socket and they are recognized by a proper code written above them. These control logics provide four different memory configurations according to J4 and J5 setting. The following paragraphs contains a graphic description of memory maps, the two jumpers setting, the used software tools and the I/O addresses.

The memory size and type is selected by some handy jumpers, as described on figure 18.

BU-1 MAP

CODE AND DATA AREA

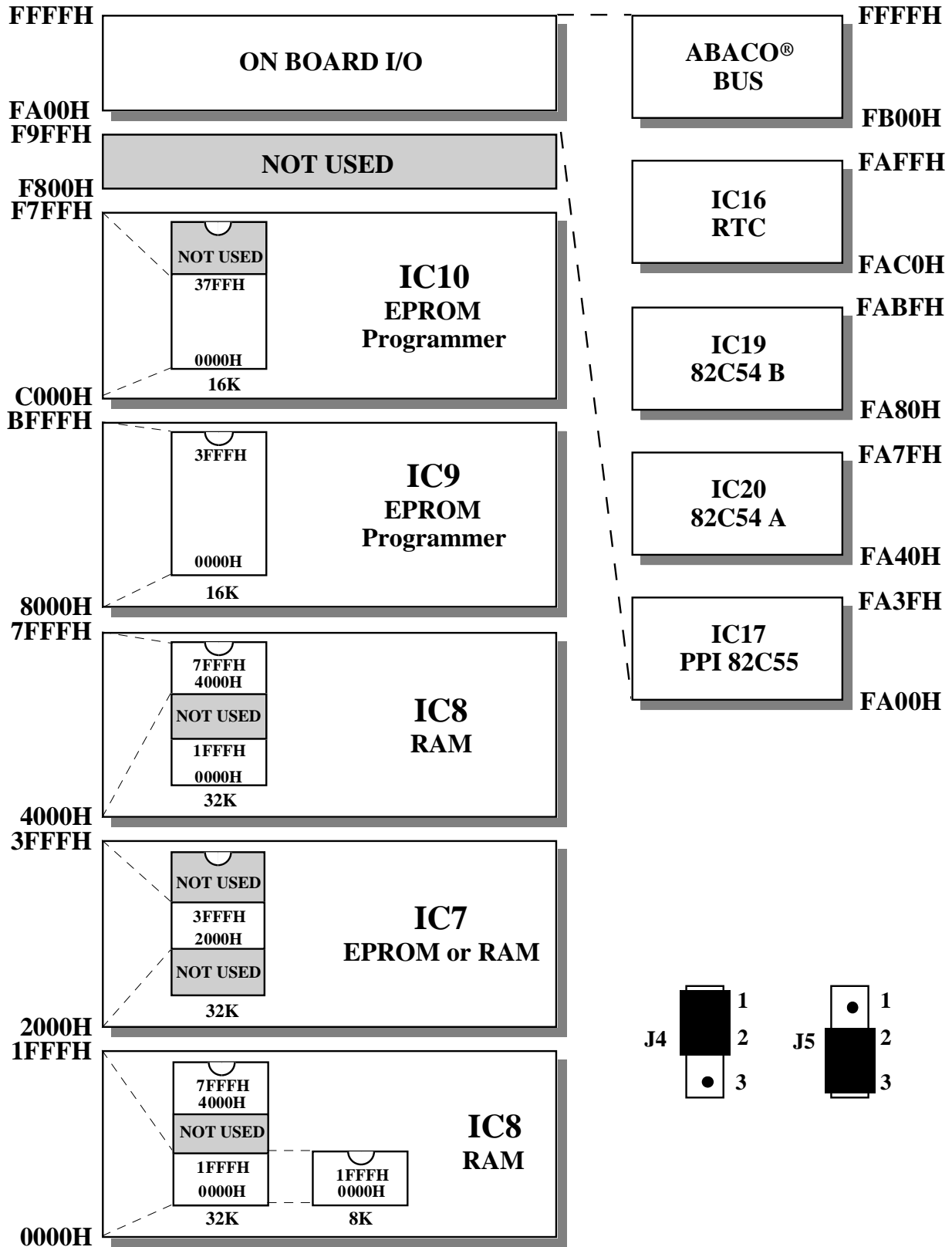


FIGURE 20: BU-1 MEMORY CONFIGURATION

Used by software tools as: BASIC F2 with utility.



BU-2 MAP

CODE AND DATA AREA

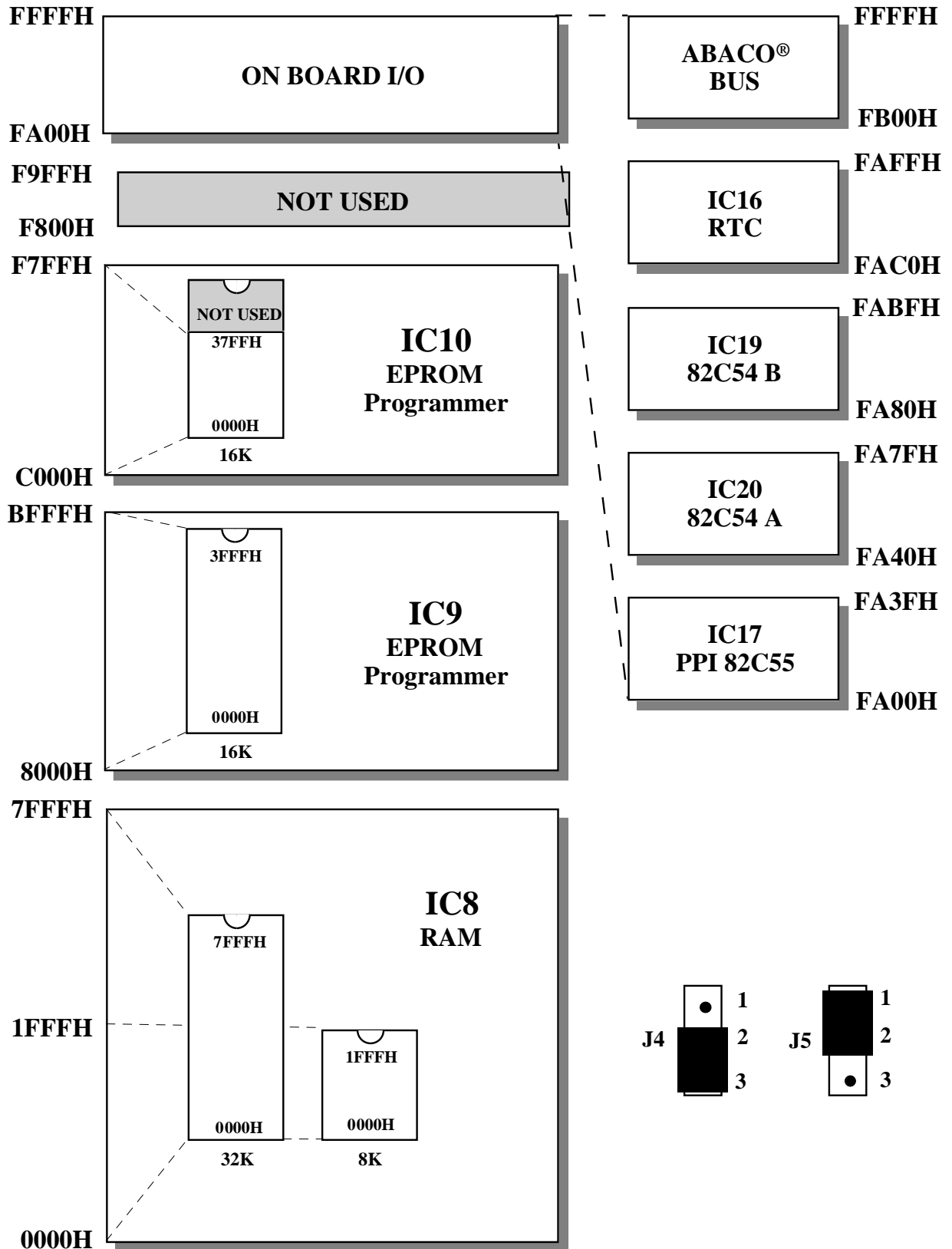


FIGURE 21: BU-2 MEMORY CONFIGURATION

Used by software tools as: BASIC F2.

BS-1 MAP

CODE AND DATA AREA

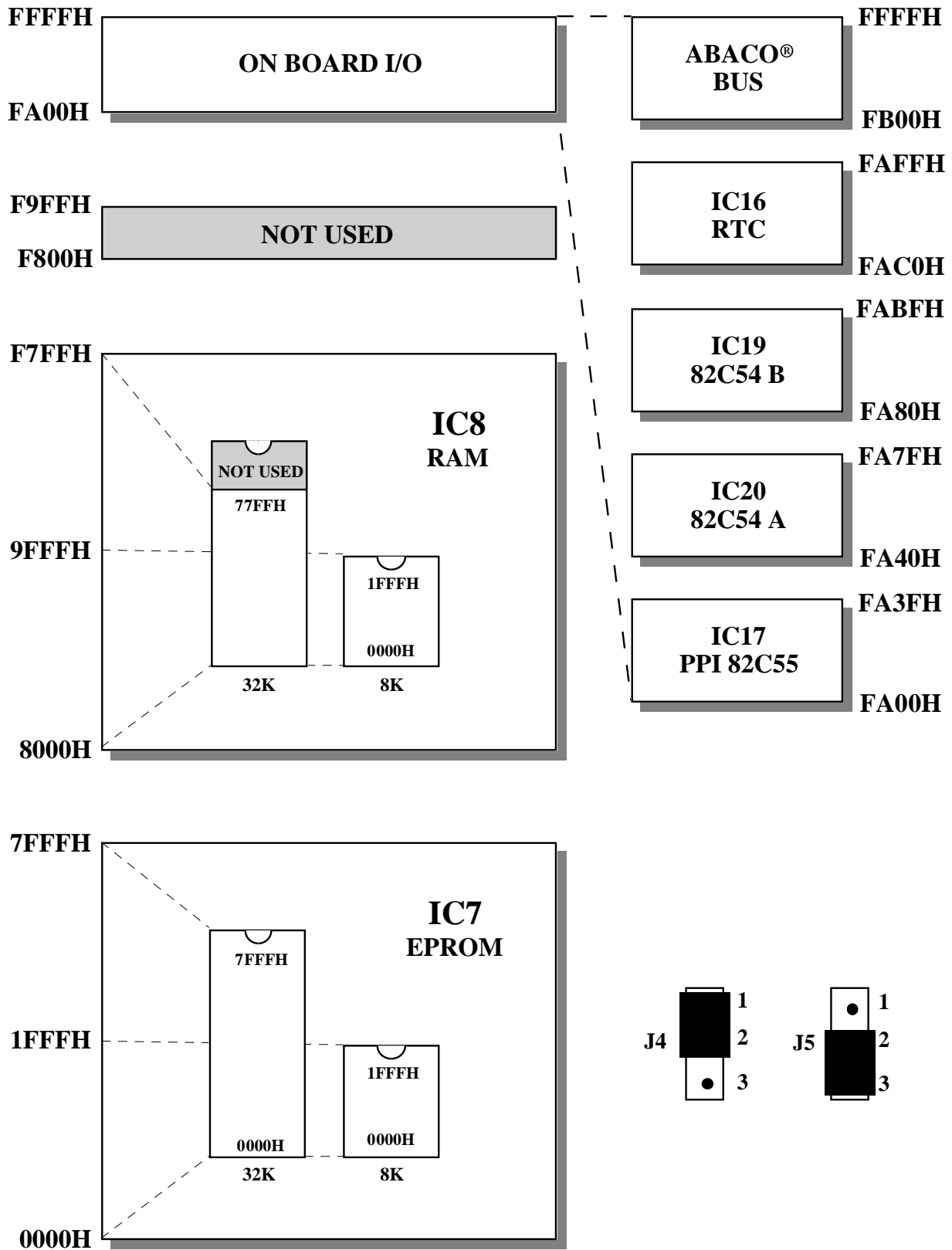


FIGURE 22: BS-1 MEMORY CONFIGURATION

Used by software tools as: BASCOM 8051; MDP; HI TECH C; DDS MICRO C; etc.  
 Note: in this configuration the IC 9 and IC 10 sockets must be empty.



BS-2 MAP

CODE AND DATA AREA

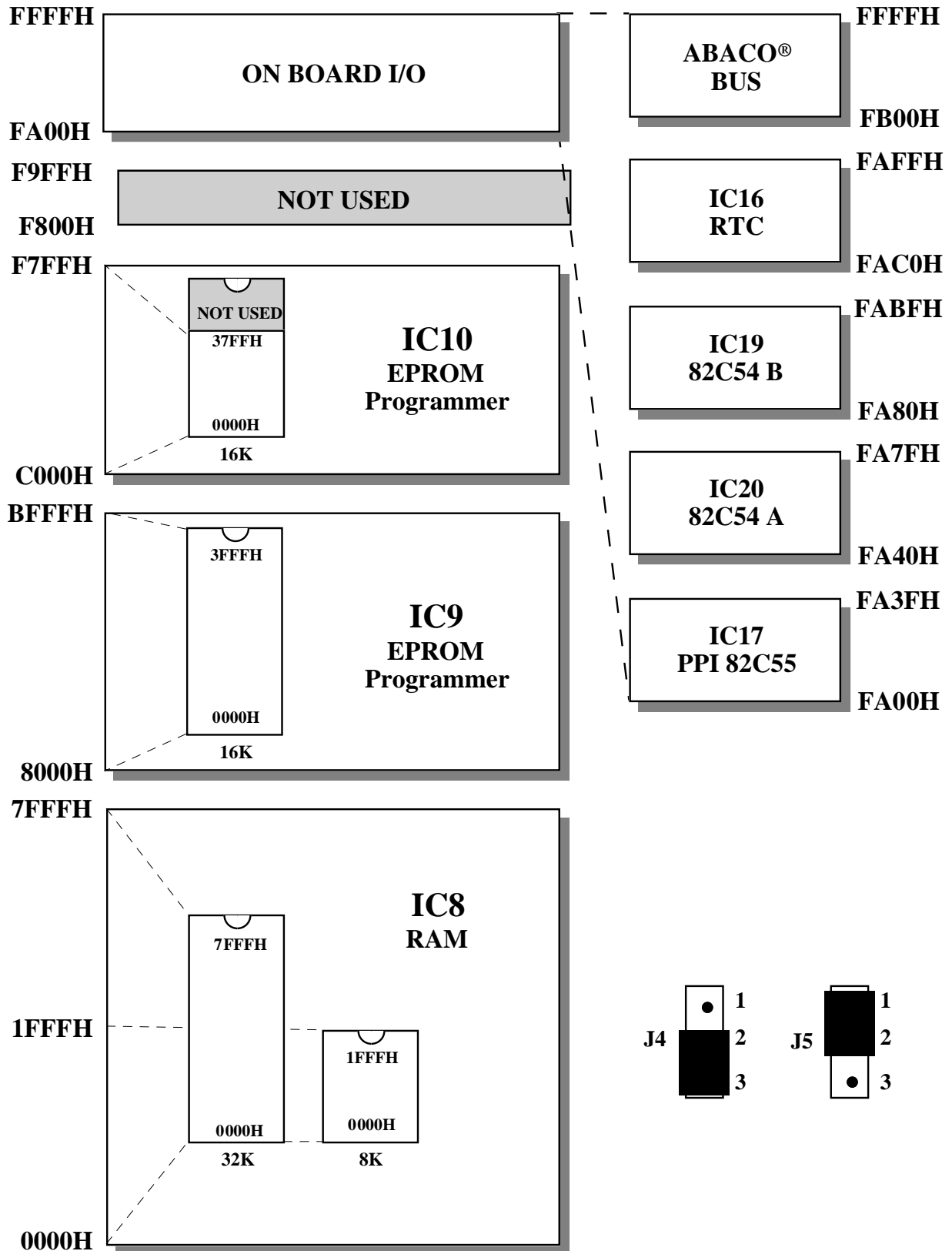


FIGURE 23: BS-2 MEMORY CONFIGURATION

Used by software tools as: BASIC F2.

## I/O ADDRESSES

I/O addresses are located in the last 1.5K bytes of the 64K bytes data and code microprocessor addressing space. Naturally memory devices can't be addressed in the space reserved for I/O addresses, in fact control logic selects only one device at a time and it excludes any conflict. Next table shows addresses, meanings and direction of peripheral devices registers (only the microprocessor external ones):

DEVICE	REG.	ADDRESS	R/W	FUNCTION
<b>PPI 82C55</b>	PDA	FA00H	R/W	Port A data register
	PDB	FA01H	R/W	Port B data register
	PDC	FA02H	R/W	Port C data register
	CNT	FA03H	R/W	Control and command register
<b>PT 82C54 A</b>	CNT0A	FA40H	R/W	Counter 0-A data register
	CNT1A	FA41H	R/W	Counter 1-A data register
	CNT2A	FA42H	R/W	Counter 2-A data register
	CWA	FA43H	W	PT 82C54 A command register
<b>PT 82C54 B</b>	CNT0B	FA80H	R/W	Counter 0-B data register
	CNT1B	FA81H	R/W	Counter 1-B data register
	CNT2B	FA82H	R/W	Counter 2-B data register
	CWB	FA83H	W	PT 82C54 B command register
<b>Real Time Clock</b>	SEC1	FAC0H	R/W	Second units data register
	SEC10	FAC1H	R/W	Second tens data register
	MIN1	FAC2H	R/W	Minute units data register
	MIN10	FAC3H	R/W	Minute tens data register
	HOU1	FAC4H	R/W	Hour units data register
	HOU10	FAC5H	R/W	Hour tens data register and AM/PM
	DAY1	FAC6H	R/W	Day units data register
	DAY10	FAC7H	R/W	Day tens data register
	MON1	FAC8H	R/W	Month units data register
	MON10	FAC9H	R/W	Month tens data register
	YEA1	FACAH	R/W	Year units data register
	YEA10	FACBH	R/W	Year tens data register
	WEE	FACCH	R/W	Day of the week data register
	REGD	FACDH	R/W	Control register D
REGE	FACEH	R/W	Control register E	
REGF	FACFH	R/W	Control register F	
<b>ABACO® BUS</b>	BUS	FB00H÷FFFFH	R/W	<b>ABACO®</b> BUS addresses

**FIGURE 24: I/O ADDRESSES TABLE**

For further information about register meanings, please refer to next chapter called "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

## PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to figure 24, for the registers name). For the microprocessor internal peripheral devices, not described in this chapter, or for further information, please refer to manufacturing company documentation.

### **STATUS LEDS**

Two of the three on board LEDs can be driven by software; in details:

- LD1 is activated when CPU P1.2 is set to 0 and viceversa;
- LD2 is activated when CPU P1.5 is set to 0 and viceversa;

Both the described signals are set to 1 after a reset or power on, mantaining disabled the LEDs.

### **BUZZER**

The BZ1 buzzer is connected to CPU P1.2 signal, thus to emit sound it is necessary to generate a PWM signal on this line. The sound type is defined by the frequency and duty cycle of this PWM signal and so it is completely software programmable. Some software tools, as BASIC F2, have high level instructions that generate this PWM signal with some software configurable parameters.

P1.2 is set to 1 after a reset or power.

### **AUXILIARY SERIAL LINE**

The auxiliary serial line available on CN3 connector is a software, monodirectional output, RS 232 buffered serial line managed through CPU P1.7 signal. The user can define either communication speed or physical protocol by changing the management software (for further information refer to software tools documentation or contact directly **grifo®**).

### **ABACO® BUS**

The **GPC® F2** control logic manages also **ABACO® BUS** interface. Through this interface it is possible to perform I/O operations on each available peripheral card. The valid addresses are those included in the range FB00H÷FFFFH, and when a peripheral card is mapped at the <baseadd> address it will be directly used with memory read and write instructions (equal to input and output intructions) at the address FB00H+<baseadd>.

## PPI 82C55

This external peripheral device is managed through 4 registers: one control and command register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for input operation (to obtain signal status) and for output operation (to set signal status) with the correspondence described in figure 24. The PPI 82C55 can work in three different modes:

*MODE 0* = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

*MODE 1* = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

*MODE 2* = it provides a 13 bits port (A+C $\div$ 7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C $\div$ 2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the control register CNT, with the following bits meaning:

<reg.> = D7 D6 D5 D4 D3 D2 D1 D0  
**CNT** = **SF M1 M2 A CH M3 B CL**

where:

SF = mode Set Flag: if activated (1) the device is enabled for standard I/O operation

M1 M2 = mode selection:

0 0 = mode 0

0 1 = mode 1

1 X = mode 2

A = port A direction: 1=input; 0=output

CH = port C HIGH direction: 1=input; 0=output

M3 = mode selection: 1=mode 1; 0=mode 0

B = port B direction: 1=input; 0=output

CL = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

When PPI 82C55 port B is connected to DIP 1 dip switch, the peripheral devices must be programmed always with this port in input; instead when DIP 1 is removed and port B is used as other 8 I/O lines, the peripheral programming must be chosen according to performed hardware connection. The correspondence between register bits and dip switches is as follows:

D7 -> DIP 1.8

D6 -> DIP 1.7

D5 -> DIP 1.6

D4 -> DIP 1.5

D3 -> DIP 1.4

D2 -> DIP 1.3

D1 -> DIP 1.2

D0 -> DIP 1.1

The data read from PDB when DIP 1 is connected is a negated combination, in fact **ON** position corresponds to **0** logic state and **OFF** position corresponds to **1** logic state.

**REAL TIME CLOCK**

This device holds 16 successive I/O locations: 3 for device status and control and 13 for data. The data registers are used with read (acquisition of actual time and date) and write (programming of new time and date) operation as well as the control registers that are read to get the RTC status or wrote to start, stop or initialize the RTC. The detailed function of all the registers is below described:

SEC1	- Second units	- Least significant 4 bits (SEC1.3÷0)
SEC10	- Second tens	- Least significant 3 bits (SEC10.2÷0)
MIN1	- Minute units	- Least significant 4 bits (MIN1.3÷0)
MIN10	- Minute tens	- Least significant 3 bits (MIN10.2÷0)
HOU1	- Hour units	- Least significant 4 bits (HOU1.3÷0)
HOU10	- Hour tens	- Least significant 2 bits (HOU10.1÷0) the third bit (HOU10.2) indicates AM/PM
DAY1	- Day units	- Least significant 4 bits (DAY1.3÷0)
DAY10	- Day tens	- Least significant 2 bits (DAY10.1÷0)
MON1	- Month units	- Least significant 4 bits (MON1.3÷0)
MON10	- Month tens	- Least significant 1 bit (MON10.0)
YEA1	- Year units	- Least significant 4 bits (YEA1.3÷0)
YEA10	- Year tens	- Least significant 4 bits (YEA10.3÷0)
WEE	- Week day	- Least significant 3 bits (WEE.2÷0)

This last register has the following meaning:

WEE.2	WEE.1	WEE.0	Week day
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

The functions of the three control registers bits are:

D7 D6 D5 D4 D3 D2 D1 D0  
**REGD = NU NU NU NU 30S IF B H**

where:

- NU = Not used.
- 30S = This bit is used to set the seconds register to 00, when placed at 1 level. If previous seconds value was greater than 29, the minutes value is increased by one.
- IF = It controls the RTC interrupt status. When the bit is read it provides the current interrupt status (1=enabled and viceversa), while if it is written to 0 it resets the interrupt request, when interrupt mode is selected (see REGE.I).
- B = This bit is used to determine whether or not data registers can be read from or written to; when it is read at 0 the data registers can be used and viceversa.
- H = When this bit is written to 1, it loads the value previously written in the data register.

D7 D6 D5 D4 D3 D2 D1 D0

**REGE = NU NU NU NU T1 T0 I M**

where:

NU = Not used.

T1 T0 = These two bits are used to define the interrupt period:

0 0 -> 1/64 second;

0 1 -> 1 second;

1 0 -> 1 minute;

1 1 -> 1 hour.

I = This bit is used to control the waveform of the interrupt output signal. There are two types of output waveform: the interrupt mode (I=1) keep the output signal in a low level until a 0 is written in REGD.IF while the standard mode keep the output signal in a low level for a fixed 7.8125 msec time.

M = This bit enables (M=0) or disables (M=1) the output interrupt signal.

D7 D6 D5 D4 D3 D2 D1 D0

**REG F = NU NU NU NU T 24/12 S R**

where:

NU = Not used.

T = This bit selects which internal counter is used for RTC counting: 1 -> main counter (fast count for testing purpose); 0 -> 15<sup>th</sup> counter (normal count).

24/12 = This bit selects the 12 or 24 hour clock mode: 1 -> 0÷23; 0 -> 1÷12 with AM/PM.

S = This bit is used to stop the RTC internal divider network (S=1) and to let it operate normally (S=0).

R = This bit is used to reset the internal counters below 1 Hz (R=1) and to release them (R=0). It does not reset any of the data registers but it reset the counter of the internal divider network.

## **PT 82C54**

Please refer to proper documentation of the manufacturing company.

## **CPU INTERNAL PERIPHERALS**

For description of the CPU internal registers and peripherals (serial lines, timers counters, watch dog, I/O ports, etc.) please refer to specific documentation of the manufacturing company.

## EXTERNAL CARDS

**GPC® F2** can be connected to a wide range of **grifo®** cards and to many system of other companies. Hereunder these cards are listed, for further information please call **grifo®** or visit web sites.

### **OBI 01 - OBI 02**

Opto BLOCK Input NPN-PNP

Interface between 16 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO®** standard I/O 20 pins connector; power supply section; connection for DIN  $\Omega$  rails.

### **OBI N8 - OBI P8**

Opto BLOCK Input NPN-PNP

Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO®** standard I/O 20 pins connector; power supply section; connection for DIN  $\Omega$  rails.

### **TBO 01 - TBO 08**

Transistor BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

### **RBO 01**

Relé BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 displayed 5A or 10A relays; screw terminal; connection for DIN  $\Omega$  rails.

### **RBO 08 - RBO 16**

Relé BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and  $\Omega$  rails.

### **XBI 01**

miXed BLOCK Input Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.

### **XBI R4 - XBI T4**

miXed BLOCK Input-Output

Interface for **ABACO®** standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and  $\Omega$  rails.

### **FBC xxx**

Flat Block Contactxxx pins

This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN  $\Omega$  rails.

**IBC 01**

## Interface Block Comunication

Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

**DEB 01**

## Didactis Experimental Board

Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, **GPC® 68** I/O connector, field connection with screw terminal.

**MCI 64**

## Memory Cards Interfaces 64 MBytes

Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any **ABACO®** I/O standard connector; High level languages GDOS supported.

**KDL xxx - KDF xxx**

## Keyboard Display interface - LCD or Fluorescent

Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by 16 TTL I/O lines; High level languages supported.

**QTP 24 - QTP 24P**

## Quick Terminal Panel 24 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

**QTP 16 - QTP 16P**

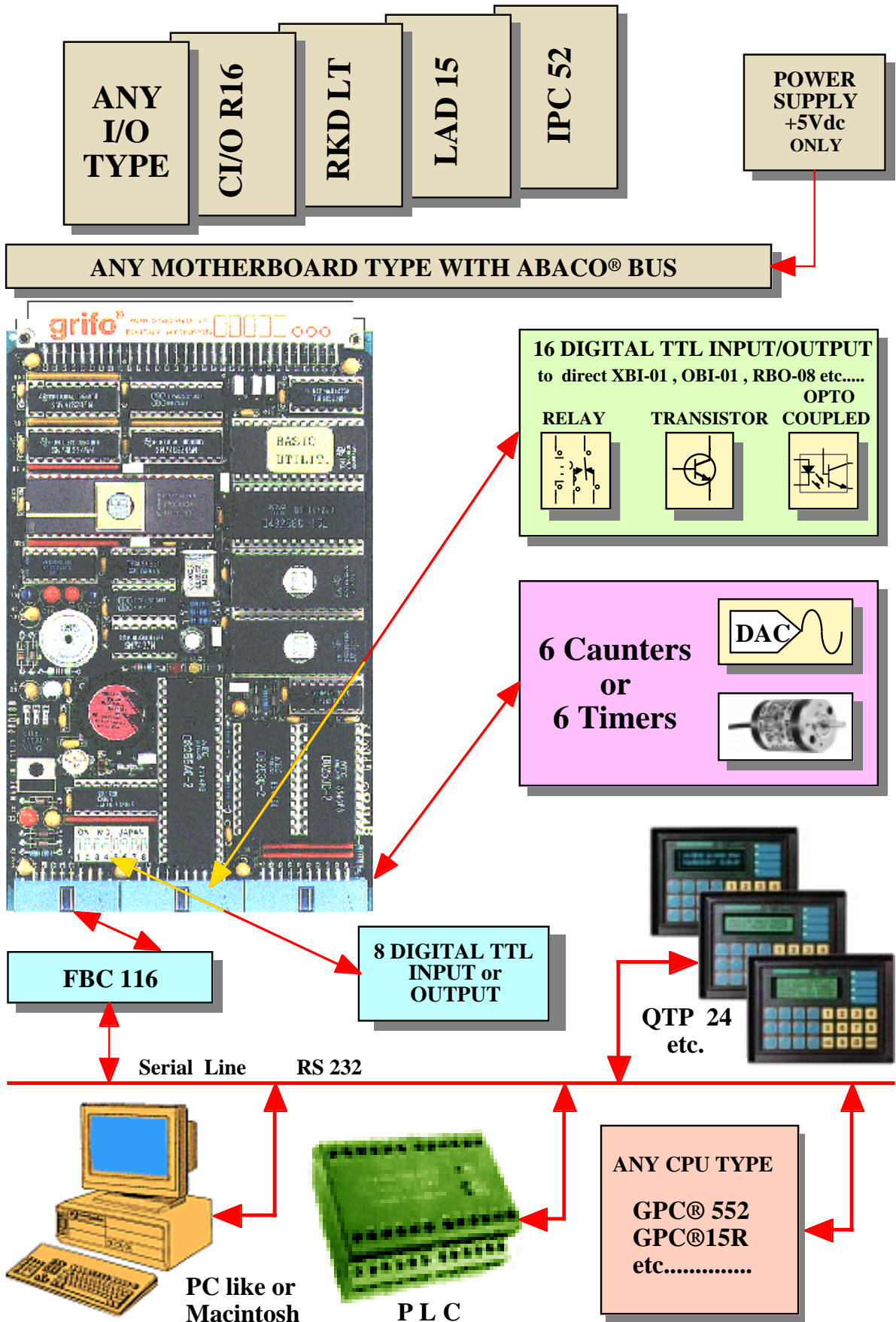
## Quick Terminal Panel 16 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and messages; buzzer manageable by software; 4 readable auxiliary opto in lines; power supply 5 Vdc. The QTP 16P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines.

**QTP G26**

## Quick Terminal Panel - LCD Graphic, 26 keys

Intelligent user panel equipped with graphic LCD display 240x128 pixel, CFC backlit; optocoupled RS 232 line and additional RS 232, RS 422, RS 485 or current loop serial line. Independent optional CAN line controller; serial E2 for set up; RTC and RAM Lithium backed; primary graphic objects; possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 26 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; reader of magnetic badge, smart-card and relay option.



**GPC®F2 Interconnections Blocks Diagram**

FIGURE 25: GPC®F2 AVAILABLE CONNECTIONS DIAGRAM

**ABB 05****ABACO® Block BUS 5 slots**

5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN  $\Omega$  rails.

**MB8 01****Mother Boards 8 slots ABACO® BUS**

8 slots **ABACO®** mother board; 5 TE pitch connectors; standard connectors for power supply and service; local reset button; 3 LEDs for power supply; direct connection on rack.

**IPC 52****Intelligent Peripheral Controller, 24 analogic input**

This intelligent peripheral card acquires 24 independent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T termocouples, 8 analog input  $\pm 2$ Vdc or  $4 \div 20$ mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

**UAR 24****Universal Analog Regulator, 2 D/A, 4 Relays**

This intelligent peripheral card for temperature PID controls, acquires 2 PT 100 sensors and 2 J,K,S,T termocouples; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; 4 conversion per second; buzzer; 4 3A relays; 2 12 bits D/A lines,  $0 \div 10$ Vdc; facility of networking up to 127 UAR 24 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

**LAD 12****Low cost Analog to Digital converter, 12 bits**

16 channels A/D converter lines; dual slope conversion; 12 bits + sign resolution; 12.5 conversion/second; range  $\pm 2.048$  V or  $0 \div 20$ ,  $4 \div 20$ mA; automatic mode functionality; 2 status LEDs; 2 TTL input lines; 8 bits BUS; normal addressing; optional front panel.

**LDA 01****Low cost Digital to Analog converter 12 bits**

Two 12 bits D/A converter; multi range  $0 \div 5$ ,  $0 \div 10$ ,  $\pm 2.5$ ,  $\pm 5$  and  $\pm 10$  V output signals; span and offset calibration; 8 digital transistor output in open collector, diplayed and optocoupled; 8 bits BUS; normal addressing; single power supply.

**C/O R16****16 Coupled Input Output with relays**

16 optocoupled inputs with low frequency filter; standard rate +24 Vdc input voltage; 16 microrelays 1 A output lines; 24 Vac noise suppressor, type MOV; I/O displayed through LEDs.

**EMI 01****Encoder Motor Interface**

Interface card for **GPC® F2** for low cost axis control solutions; 3 optocoupled acquisition lines for bidirectional incremental encoders; direction identifier; phases multiplier; 2 D/A sections based on PWM signals; standard connectors.

## BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® F2**.

Data book TEXAS INSTRUMENTS:	<i>The TTL Data Book - SN54/74 Families</i>
Data book TEXAS INSTRUMENTS:	<i>Linear Circuit Data Book - Volume 1 and 3</i>
Data book TEXAS INSTRUMENTS:	<i>Mos Memory Data Book</i>
Data book NEC:	<i>Microprocessor and Peripherals - Volume 3</i>
Data book NEC:	<i>Memory Products</i>
Data book MAXIM:	<i>New Releases Data Book - Volume 4</i>
Data book PHILIPS:	<i>80C51 - Based 8 Bit Microcontrollers</i>
Data book DALLAS SEMICONDUCTOR:	<i>1992-1993 Product Data Book Supplement</i>
Data book NATIONAL SEMICONDUCTOR:	<i>Linear Data Book - Volume 1</i>
Data book INTEL:	<i>8 Bit Embedded Microcontrollers</i>
Documentation OKI ELECTRIC:	<i>Microprocessor real time clock calendar</i>

For further information and upgrades please refer to specific internet web pages of the manufacturing companies.



## APPENDIX A: CARD ASSEMBLY

The **GPC® F2** can be ordered in two different mode: completely mounted, tested and ready to use or in assembly kit. In this final condition the user can directly use the information of this chapter.

### COMPONENTS LIST

In the following paragraphs there are the components lists divided according with the card sections. Please remember that only the base component are really necessary, while all the others are options and they can be mounted only if required by the user.

### **BASE COMPONENTS**

#### *Soldered:*

BZ1 - Passive piezo electric buzzer.

CN3 - 16 pins, 90°, low profile connector.

C1, C2, C15, C16, C19, C27, C37 - 22  $\mu$ F 6,3V tantalum capacitor .

C3, C4, C5, C6, C7, C8, C9, C10, C13, C14, C20, C21, C22, C28 - 100 KpF multi layered capacitor.

C11, C12 - 22 pF NP0 ceramic capacitor.

C17, C18 - 22  $\mu$ F 16V tantalum capacitor.

D1, D3 - 1N4148 diode.

IC1, IC2, IC4, IC5 - 20 pins, d.i.l., low profile socket.

IC3, IC11, IC18 - 16 pins, d.i.l., low profile socket.

IC6 - 40 pins, d.i.l., low profile socket.

IC7, IC8, IC9, IC10 - 28 pins, d.i.l., low profile socket.

IC12, IC13, IC14 - 14 pins, d.i.l., low profile socket.

J1, J8 - 2 pins , 2.54 mm pitch, male strip.

J2, J3, J4, J5, J6 - 3 pins , 2.54 mm pitch, male strip.

K1 - DIN 41612, 64 pins, 90°, male, case C, type A+C connector (fixed with 2 screw).

LD1 - 3 mm yellow LED.

RR1, RR2, RR3, RR4, RR5 - 10 K $\Omega$ , 10 pins (9 commoned) resistor network.

R10 - 10 K $\Omega$ , 1/4 W resistor.

R7 - 47 K $\Omega$ , 1/4 W resistor.

R12 - 270  $\Omega$ , 1/4 W resistor.

XTL1 - 11.0592 MHz, HC49 crystal.

#### *On socket:*

IC1, IC5 - 74 LS 245.

IC4 - 74 HCT 245.

IC2 - 74 LS 373.

IC3 - N82S123 burned model "BS" or "BU".

IC18 - N82S123 burned model "18".

IC6 - CPU 8052 AH BASIC, 80C32, 80C320 etc.

IC7 - RAM D4364 (8K), EPROM 27c64 (8K) or 27c256 (32K).

IC8 - RAM D4364 (8K) or D43256 (32K).

IC9, IC10 - EPROM 27c64 (8K) or 27c128 (16K).

IC11 - MAX202.

IC12 - 74 HCT 08.

IC13 - 74 HCT 14.

IC14 - 7407.

Jxx - 8 two pins female jumpers for male strip.

**PT 82C54 COMPONENTS**

*Soldered:*

CN1 - 20 pins, 90°, low profile connector.

C29, C30 - 100 KpF multi layered capacitor.

C39 - 22 µF 6,3V tantalum capacitor.

IC19, IC20 - 24 pins, d.i.l., low profile socket.

R8, R11 - 10 KΩ, 1/4 W resistor.

RR7, RR8 - 10 KΩ, 10 pins (9 commoned) resistor network.

*On socket:*

IC19, IC20 - PT 82c54.

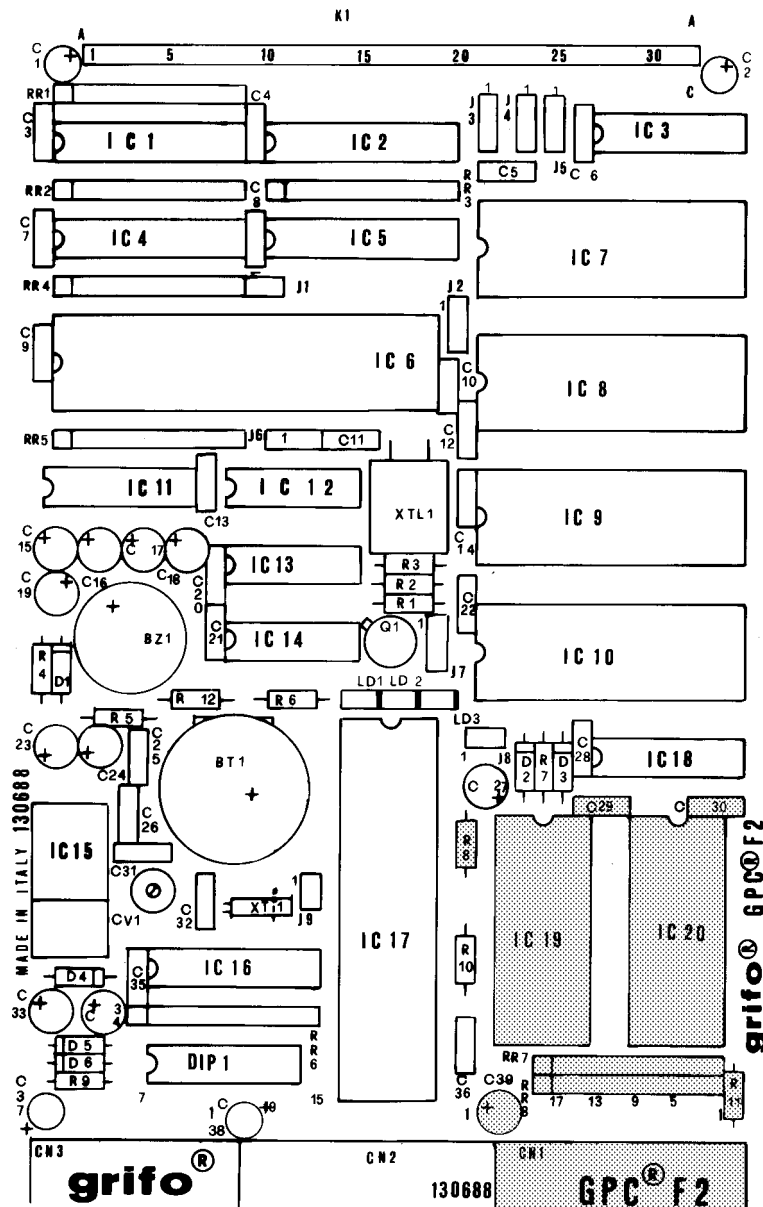


FIGURE A-1: COMPONENTS MAP FOR PT 82C54 SECTION



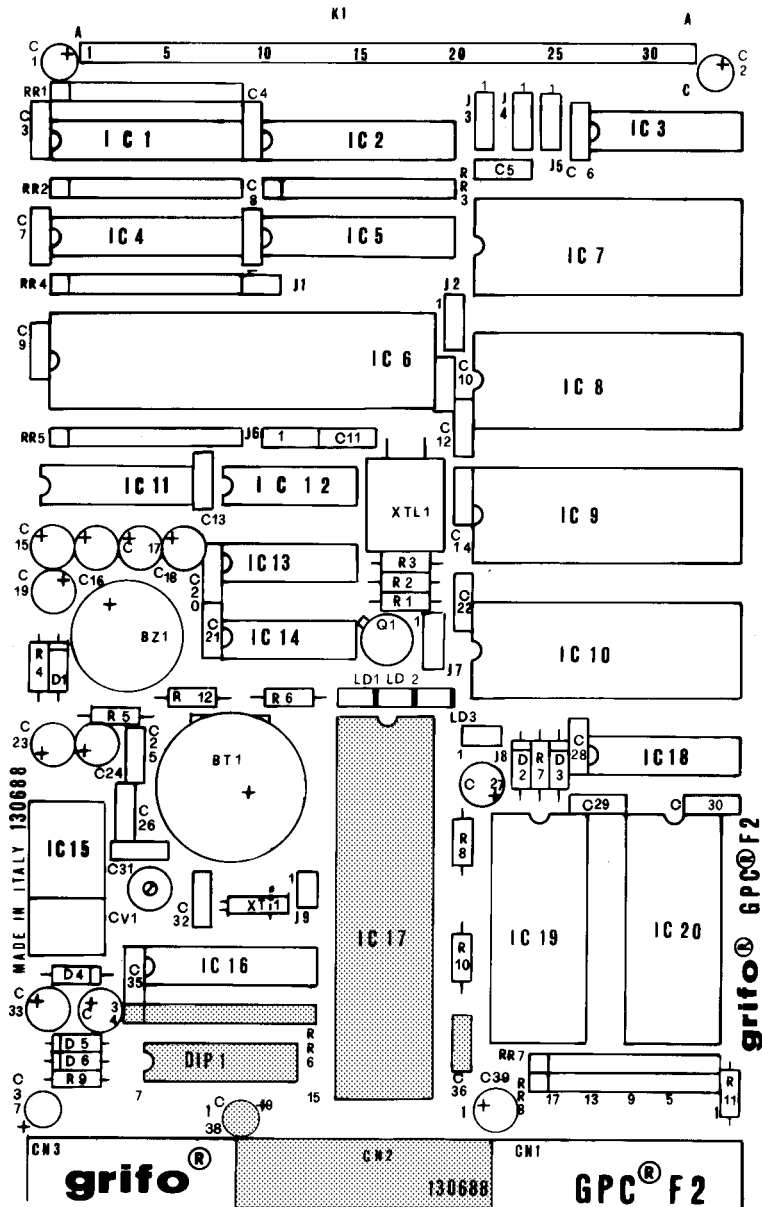
**PPI 82C55 COMPONENTS**

*Soldered:*

- CN2 - 20 pins, 90°, low profile connector.
- C36 - 100 KpF multi layered capacitor.
- C38 - 22 µF 6,3V tantalum capacitor.
- DIP 1 - 16 pins, d.i.l., low profile socket.
- IC17 - 40 pins, d.i.l., low profile socket.
- RR6 - 10 KΩ, 10 pins (9 commoned) resistor network.

*On socket:*

- IC17 - PPI 82c55.
- DIP1 - 8 SPST dip switch.



**FIGURE A-2: COMPONENTS MAP FOR PPI 82C55 SECTION**



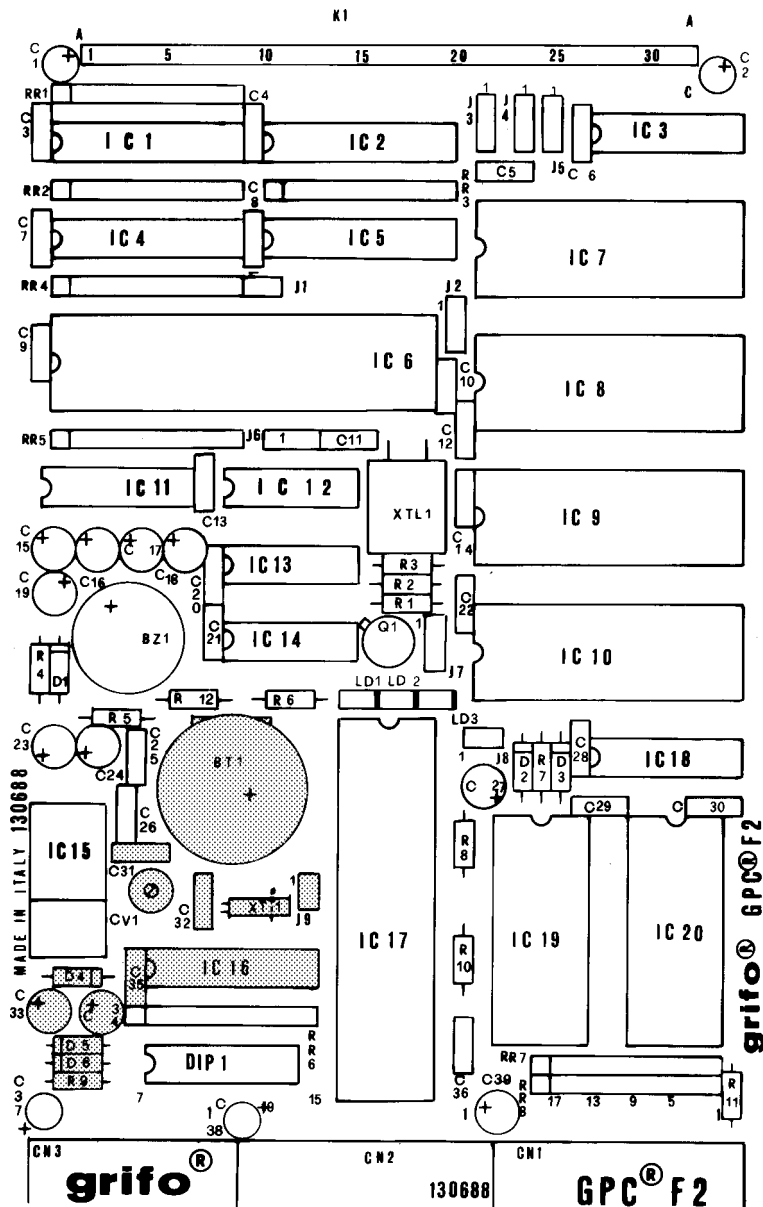
**RTC COMPONENTS**

*Soldered:*

- CV1, C31 - 22 pF NP0 ceramic capacitor.
- C32 - 4,7 pF NP0 ceramic capacitor.
- C33,C34 - 22 µF 6,3V tantalum capacitor.
- C35 - 100 KpF multi layered capacitor.
- BT1 - 3V or 3.6V lithium battery, tipe TADIRAN TL586 or SAFT LM 2032 90°
- D4, D5, D6 - 1N4148 diode.
- IC16 - 18 pins, d.i.l., low profile socket.
- J9 - 2 pins , 2.54 mm pitch, male strip.
- R9 - 47 KΩ, 1/4 W resistor.
- XT1 - 32.384 KHz, cylindrical crystal (fixed with wire).

*On socket:*

- IC16 - OKI M6242B.



**FIGURE A-3: COMPONENTS MAP FOR RTC SECTION**



**EPROM BURNING COMPONENTS**

*Soldered:*

- C23 - 22 µF 6,3V tantalum capacitor.
- C24 - 22 µF 25V radial wire electrolytic capacitor.
- C25, C26 - 100 KpF multi layered capacitor.
- D2 - 1N4148 diode.
- IC15 - LM7806, TO220 case, voltage regulator.
- J7 - 3 pins , 2.54 mm pitch, male strip.
- LD2 - 3 mm red LED.
- LD3 - 3 mm green LED.
- Q1 - 2N2907 transistor.
- R1, R2, R3 - 10 KΩ, 1/4 W resistor.
- R4 - 1 KΩ, 1/4 W resistor.
- R5 - 820 Ω, 1/4 W resistor.
- R6 - 330 Ω, 1/4 W resistor.

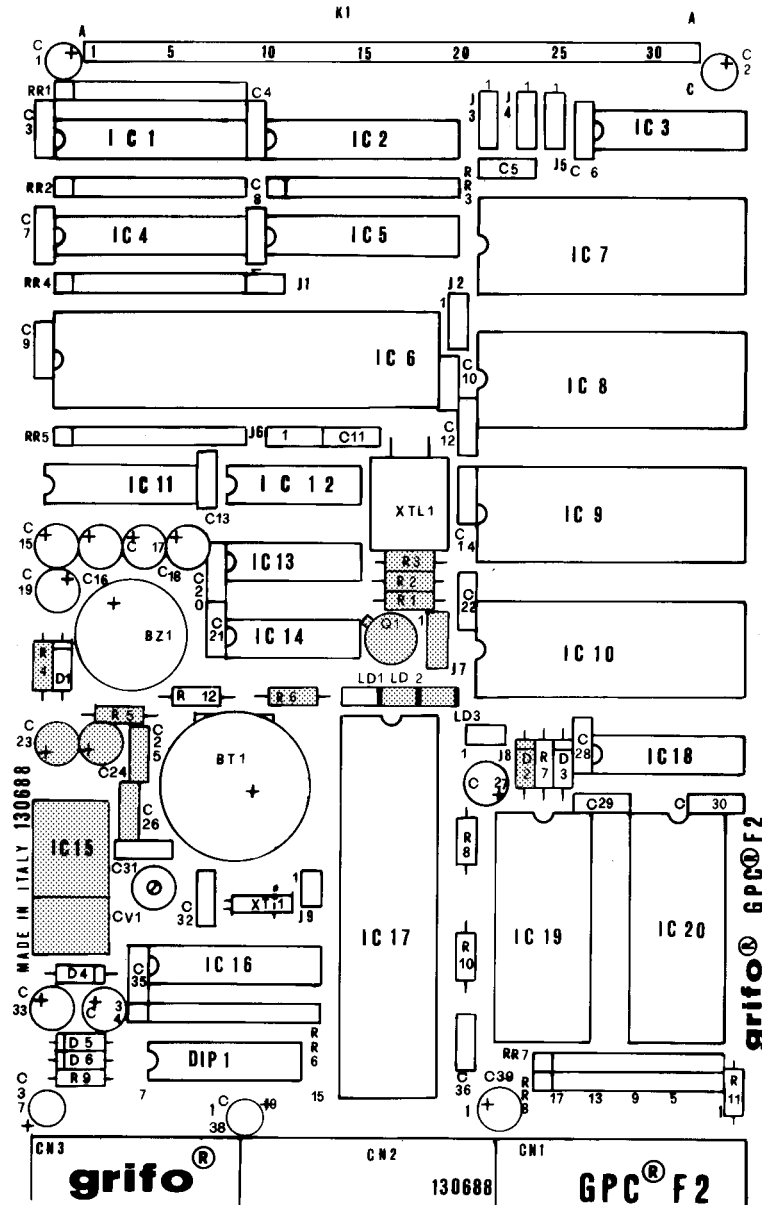
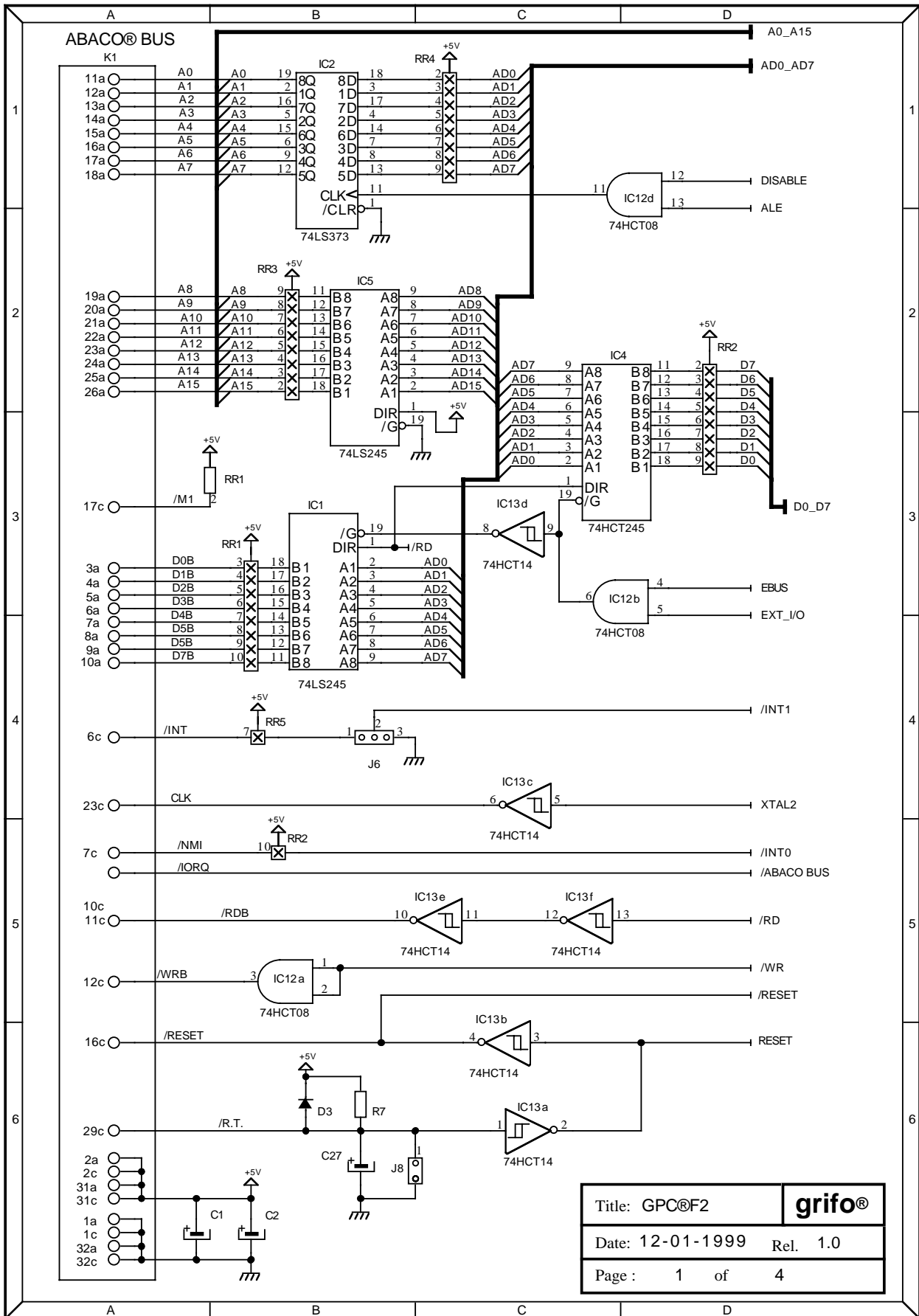


FIGURE A-4: COMPONENTS MAP FOR EPROM BURNING SECTION



**ELECTRIC DIAGRAM**



**FIGURE A-5: ELECTRIC DIAGRAM 1 OF 4**



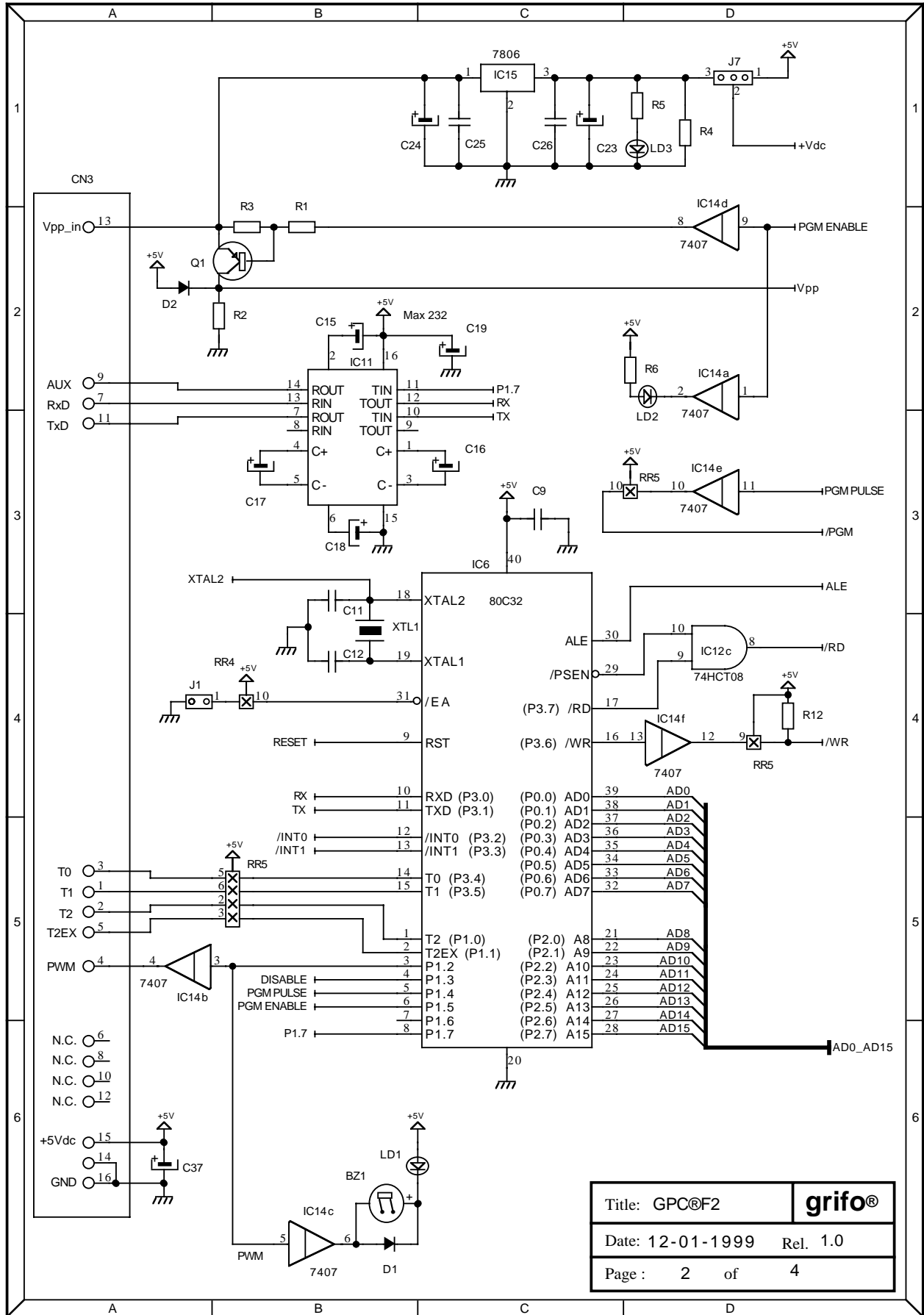
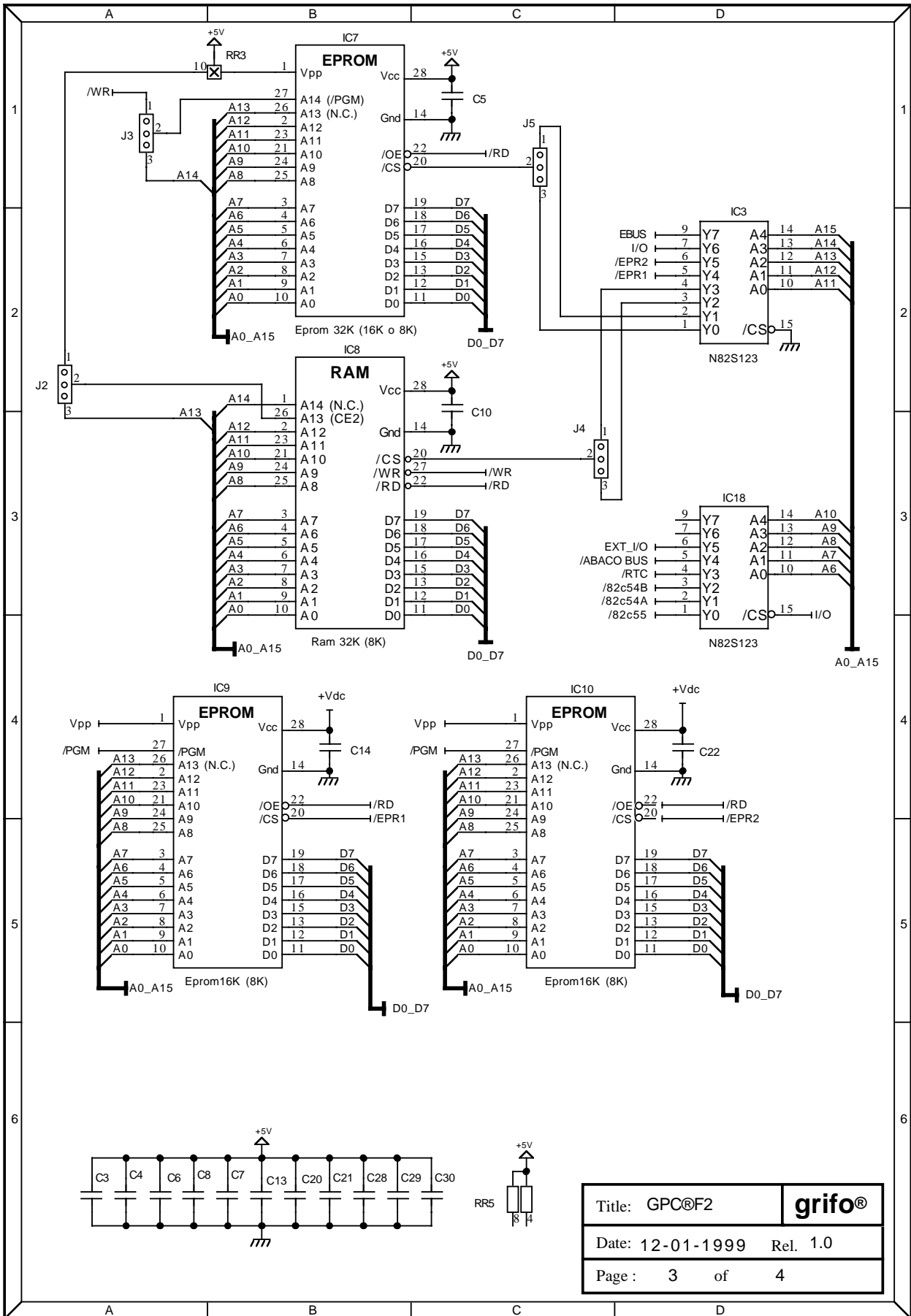


FIGURE A-6: ELECTRIC DIAGRAM 2 OF 4

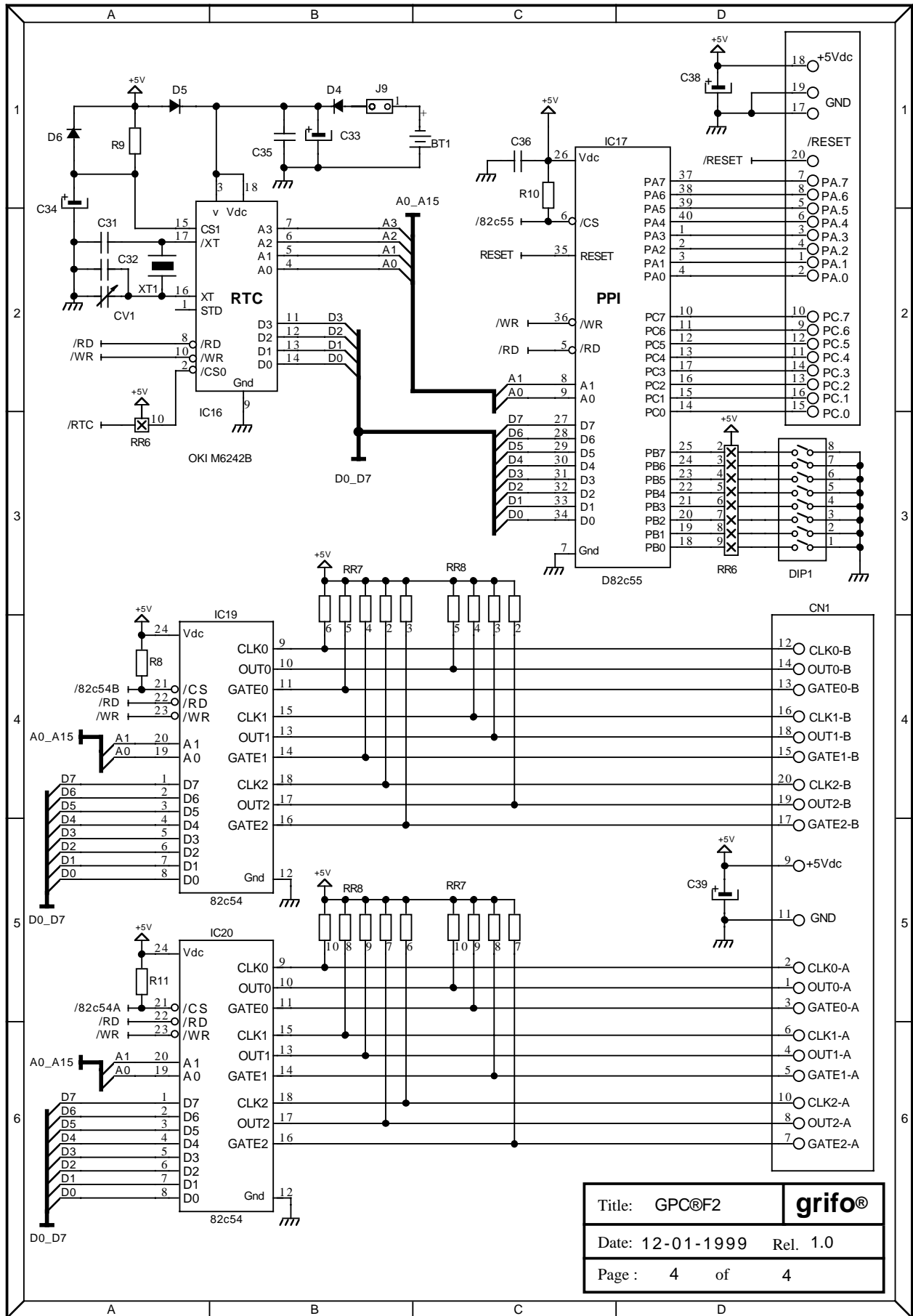




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FIGURE A-7: ELECTRIC DIAGRAM 3 OF 4





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FIGURE A-8: ELECTRIC DIAGRAM 4 OF 4





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